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OPERATION & MAINTENANCE HANDBOOK

MODEL 225-S30453

MODEM TEST SET

TASK DATE NONE

SYSTRON-DONNER CORPORATION



10150 W. Jefferson Blvd., Culver City, Calif. 90230
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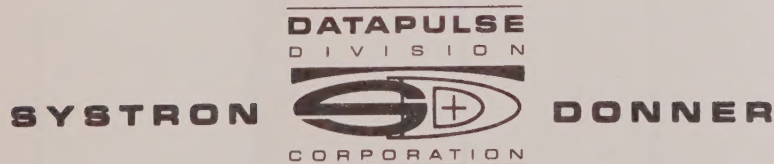
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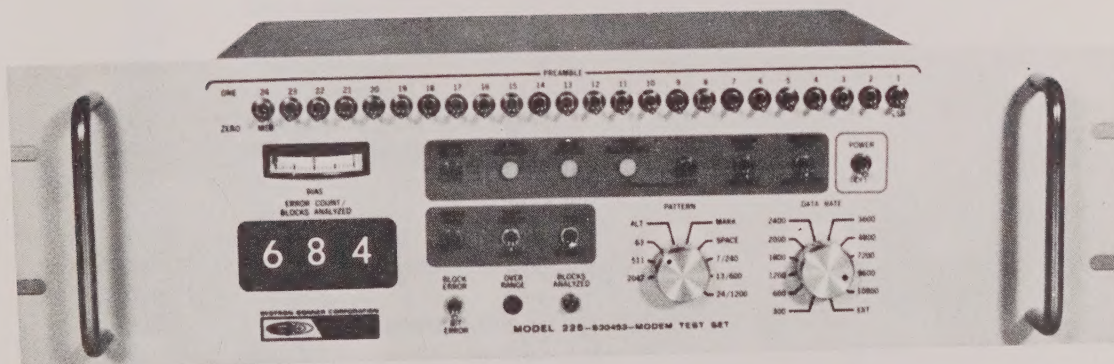


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1.0 INTRODUCTION

The DATAPULSE Model 225 Modem Test Set is a completely self-contained, portable instrument used to determine the bit error rate, block error rate, and bias distortion of both synchronous and asynchronous data communications systems, multiplexers, and modems.

The test set contains both a data generator (transmitter) and a data analyzer (receiver). In application, a known bit pattern is generated, transmitted through the communication equipment under test, received and then analyzed for bit error rate, block error rate and bias distortion. The number of blocks or bits in error as well as the number of blocks analyzed are displayed on direct readout indicators. The test may be employed end-to-end or loop-back since the device has full duplex capability.

The Model 225 generates six patterns, three of which are classed as pseudo-noise sequences required to determine data transmission performance and three of which are levels and level reversals required to determine bias distortion. The variety of test patterns allow compatibility with Western Electric, International Data Sciences, and other transmission test sets that conform to CCITT recommendations.

When externally timed for synchronous applications, the Model 225 is capable of operating at data rates up to half a megahertz. For asynchronous applications, the timing is internally generated with a high stability crystal-controlled oscillator providing selectable data rates of 75, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, and 9600 bits per second. Other data rates are optionally available.

Additional features include Invert Data, Transmit (Xmit) Errors, Break Sync, Clock Monitor indicator, Sync Locked indicator and Sync Recovered indicator capability.

The Invert Data switch may be used to invert the transmitted data to compensate for transmission or receiver constraints, to allow link-up with test equipment that utilizes inverted maximal length pseudo-noise sequences, or to determine independency of test results on signal polarity.

The Xmit Errors switch may be used to allow error insertion at the transmitter and observation of that error at the receiver, providing a positive indication that data transfer and performance analysis is occurring.

The Break Sync pushbutton, Sync Locked indicator and Sync Recovered indicator allow verification of test synchronization. The Clock Monitor indicator displays the status of the received clock in synchronous operation and the internally generated receiver clock in asynchronous operation.

In addition to the standard RS232 interface for interconnection with the modem, there is an auxiliary connector on the rear panel allowing access to the display count signals, the error pulse signal, transmitter and receiver pattern sync pulses, and others. These signals are made available to facilitate more sophisticated testing and/or test recording. The printer option (DATAPULSE Model 5000 Test Set Printer) plugs into this connector to provide a permanent record copy of test results.

As an option, the Model 225 may be supplied with a Dual Data Rate selector, a Block Length selector, additional data rates, signal monitoring capability, special logic levels and a leather carry case. Many

other options are listed and described in Sections 7.0 and 11.0. The unit is portable, lightweight and rugged, featuring simple operation while performing sophisticated tests. Both desk-top and rack-mount configurations are available.

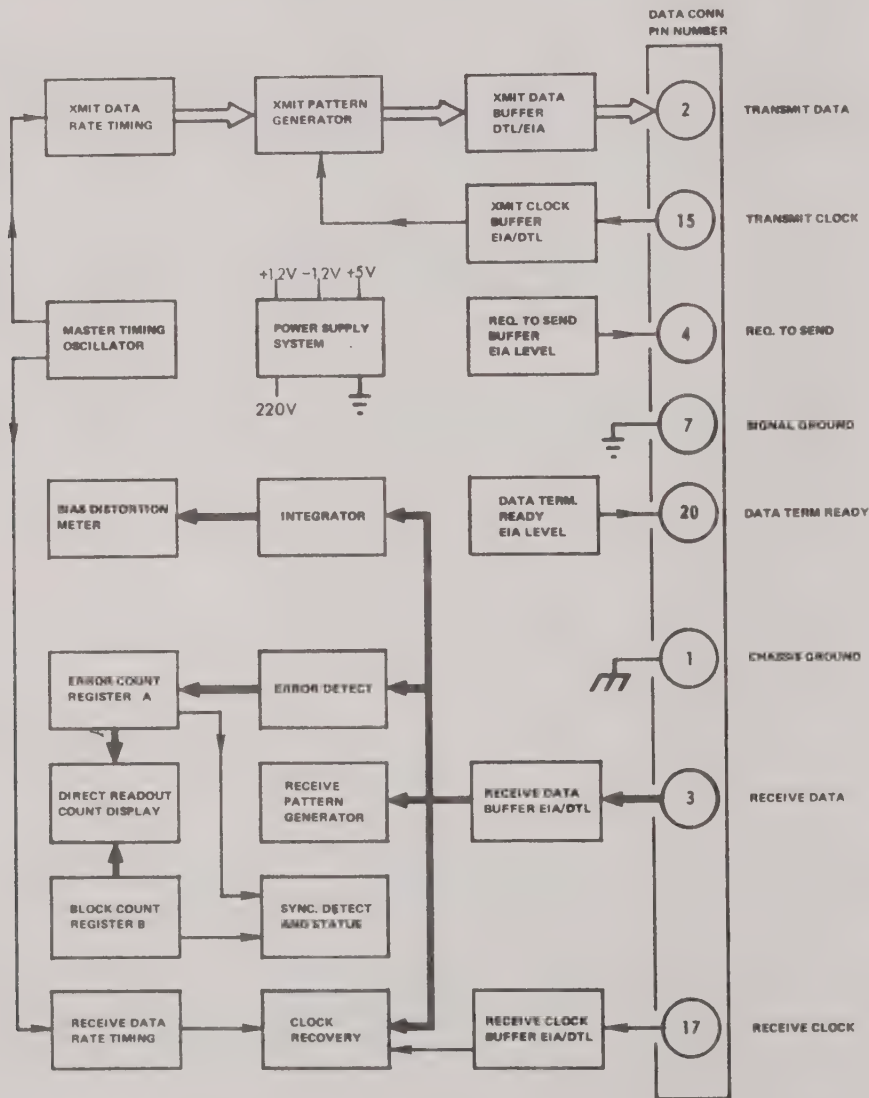


Figure 1. Model 225 System Block Diagram

2.0 MODEL 225 OPERATION

Each Model 225 Modem Test Set is comprised of an independent Data Generator (Transmitter) and Data Analyzer (Receiver) as illustrated in the system block diagram of Figure 1.

The Transmitter portion is capable of generating any of six selectable data patterns or their inverse for use in evaluating the transmission capability of the communication system under test.

If timing is supplied by the modem, the transmitter will generate the selected data at rates of up to half a megahertz (higher data rates are optionally available). For modems that do not supply timing, the data rates internal to the transmitter may be selected by a front panel control (additional data rates are optionally available). The data is buffered to standard EIA levels per RS232 and supplied to a Data Connector located on the rear panel (MIL 188, DTL/TTL, or other interface levels are optionally available).

The Receiver portion is capable of analyzing the received pseudo-noise data patterns for bit error rate and block error rate, or analyzing the received alternate mark/space pattern for bias distortion. Data received at the data connector is buffered through EIA double threshold hysteresis circuits before analysis.

To allow bias distortion measurements, the buffered Receive Data is processed through a mark/space duration integrator and the results displayed on a front panel meter. Details are described in the applications section of this manual.

To allow bit error rate or block error rate measurements, the buffered Receive Data signal is synchronized to a locally generated reference sequence and compared bit-by-bit for transmission errors. Bits or blocks in error are counted in Register A and displayed by direct readout on the front panel. The number of blocks analyzed are counted in Register B and may be displayed on the same front panel readout by depressing the pushbutton labeled Blocks Analyzed. A block of data is defined to be one pseudo-noise word, and therefore contains 2047, 511, or 63 bits. A block length selector switch is optionally available allowing the block length to be defined as binary multiples of the selected word or integral powers of 10 ranging from 10^3 bits to 10^8 bits (see option list).

3.0 SELF TEST CAPABILITY

The Model 225 Test Set can be completely and conveniently checked to determine if it is operating correctly by means of two toggle switches and a pushbutton on the front panel. The Test-Operate switch allows the transmitter to be looped around to the receiver, testing the automatic synchronization, clock recovery, clock monitor and buffer circuits. The Break Sync pushbutton allows a forced break in synchronization between the transmitter and the receiver, testing sync lost detection circuitry, automatic resynchronization circuitry and the sync status circuitry. The Xmit Errors switch allows one error per pseudo-noise word to be transmitted, testing the error detection and error display circuitry. All of these tests can be performed without disconnecting the test set from the modem. To perform the above tests, the Pattern selector switch must be in either the 2047, 511, or 63 bit pseudo-noise position. Selecting the Mark, the Alternate Mark/Space, and the Space positions will facilitate testing the Bias Meter positions labeled "M", "O", and "S", respectively.

4.0 CONSOLE INDICATORS

The following console indicators are located on the front panel of the Model 225 Modem Test Set.

4.1 Three Digit Decimal Display

During bit error rate testing, these indicators provide a direct readout of the number of bits in error. During block error rate testing, these indicators provide a direct readout of the number of blocks in error. When the pushbutton labeled Blocks Analyzed is depressed, these indicators provide a direct readout of the number of blocks analyzed during the error rate tabulation.

4.2 Overrange

Provides a warning indication when the quantity being displayed by the decimal display has exceeded 999.

4.3 Bias Meter

Provides a measure of Mark/Space bias distortion in the received data signal. The meter is calibrated in percent and labeled "M" at the left end indicating 100% Mark distortion, "S" at the right end indicating 100% Space distortion, and "O" at the center indicating no Mark/Space distortion. Intermediate markings are at the 10% increments.

4.4 Clock Monitor

Indicates when a clock signal is present at the receiver. When the Data Rate selector switch is in the EXT position, the Clock Monitor indicates the presence of a Receive Clock signal. When the Data Rate selector switch is in a selected internal timing position, the Clock Monitor indicates the presence of that internal timing signal.

4.5 Sync Locked

Indicates that the pseudo-noise pattern generated in the receiver is in synchronization with the data signal being received for error rate analysis.

4.6 Sync Recovered

Indicates that the receiver has detected a loss of synchronization during the test, automatically resynchronized, and has started a new test.

5.0 CONSOLE CONTROLS

The following console controls are located on the front panel of the Model 225 Modem Test Set.

5.1 Bit Error/Block Error

In the Bit Error position, bit-by-bit differences between the Receive Data signal and the locally generated pseudo-noise sequence are counted. In the Block Error position, block-by-block differences (one or more errors in a block is defined as a block difference) between the Receive Data signal and the locally generated pseudo-noise sequence are counted. No counting occurs when Mark, Space, or Alternate Mark/Space is selected on the pattern switch. Error analysis on the Alternate Mark/Space pattern is available as an option.

5.2 Reset Count

This pushbutton resets the error counter, the block counter, and their respective overrange storages.

5.3 Break Sync

This pushbutton causes the receiver to become non-synchronized with the receive data signal. Allows self-test of sync loss detection and auto-resynchronization circuitry in the Bit Error or Block Error modes.

5.4 Invert Data

A toggle switch that allows the inverted data pattern to be transmitted and received. Facilitates link-up with test gear transmitting the inverted maximal length sequence. Also allows the determination of test result dependency on signal polarity.

5.5 Xmit Errors

A toggle switch that causes the insertion of one error per pseudo-noise sequence to be transmitted. Detection of the error at the receiver provides a positive indication that data transfer and error analysis is occurring.

5.6 Test-Operate

In the Test position, the transmitter data is directed to the receiver input terminal. Self-test of the transmitter and receiver then takes place at a rate determined by the Data Rate selector switch. This mode will allow operation of the Model 225 independent of external equipment to test its operation. In the Operate position, the Model 225 is conditioned for the normal operation; communication link, multiplexer or modem testing.

5.7 Receive Only—Trans/Rec

When the toggle switch is in the Receive Only position, the Request to Send signal is off. The Model 225 is then conditioned to receive data, synchronize, and count errors or to perform bias distortion measurements. When the toggle switch is in the Trans/Rec position, the Request to Send signal is ON. The Model 225 is then conditioned to transmit the selected data pattern and to receive data, synchronize, and count errors or perform bias distortion measurements.

5.8 Blocks Analyzed

This pushbutton causes the number of blocks analyzed for errors to be displayed and the overrange to indicate when more than 999 blocks have been analyzed. Releasing the pushbutton allows the decimal display to return to its error count display and overrange to indicate when more than 999 errors have been counted.

5.9 Data Rate

Bit rate selections of 75, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200 and 9600 are standard for asynchronous operation; i.e., the timing is not supplied by the modem. Select EXT for synchronous operation; i.e., the timing is supplied by the modem.

5.10 Pattern

Pattern selections are 2047, 511, and 63 indicating the length of maximal length pseudo-noise sequences; and all Mark, all Space, and Alternate Mark/Space sequences for bias distortion measurements.

5.11 Power On

The power switch energizes and automatically initializes the unit including its counters and sync status circuitry.

6.0 SPECIFICATIONS AND INTERFACE

6.1 Power

115 or 230 V ac $\pm 10\%$, 50–60 Hz. Approximately 35 watts. Details of power strapping changes are given in Section 9.0.

6.2 Operating Temperature

0° C to 50° C.

6.3 Size

Desktop: 12½" W x 4" H x 8-5/8" D. Rack Mount: 19" W x 4" H x 8-5/8" D.

6.4 RS232 Interface

All signals conform to RS232/CCITT V 24 specifications. A Data Connector is mounted on the back panel. Signals are listed in Table 1.

The input signals are Received Data, Transmitter Clock, and Receiver Clock, all required to be below level and polar, suitable for use with electronic circuitry. In the Test Set, these signals are processed through double threshold hysteresis circuits to allow high noise immunity.

Table 1. Data Connector

Connector Pin	CCITT V 24 Designation	RS232 B or C Designation	Title	Description Note: "ON" = Positive voltage = Space = Binary 0; "OFF" = Negative voltage = Mark = Binary 1
1	101	AA	Protective Ground	This lead is an electrical equipment frame and power ground.
2	103	BA	Transmitted Data (TD)	This lead carries the signals that originate in the test set and are to be transmitted by the data modem to a distant station. An output from the test set.
3	104	BB	Received Data (RD)	This lead carries the signals that are generated by the data modem in response to signals from a distant station. An input to the test set.
4	105	CA	Request to Send (RTS)	An "on" condition on this lead indicates that the test set is ready to transmit data. An output from the test set.
5*	106	CB	Clear to Send (CTS)	An "on" condition on this lead indicates that the data modem is ready to transmit data from the test set to a distant terminal. An input to the test set used only with signal monitoring options.
6*	107	CC	Data Set Ready (DSR)	An "on" condition on this lead indicates that the modem is ready to process data. An input to the test set used only with signal monitoring options.
7	102	AB	Signal Ground	This lead establishes the common ground reference potential for all circuits except protective ground.
8*	109	CF	Receive line Signal (Data Carrier) Detector (DCD)	This lead provides an indication that data carrier signals from the remote station are being received by the modem. An input to the test set. Used only with Signal Monitoring options.
9-11*				Not used.

*These leads are not normally included in cable supplied with test set, unless unit is equipped with the options specified.

Table 1 (cont.)

12*	122	SCF	Secondary Receive Line Signal (Data Carrier) Detector (DCD)	This lead provides an indication that data carrier signals from the remote station on the secondary channel are being received by the modem. An input to the test set used only with signal monitoring options.
13*	121	SCB	Secondary Clear to Send (CTS)	An "on" condition on this lead indicates that the data modem is ready to transmit data on the secondary channel from the test set to a distant terminal. An input to the test set used only when both the Signal Monitoring and Dual Data Rate options are installed.
14*	118	SBA	Secondary Transmitted Data (TD)	This lead carries the signals that originate in the test set and are transmitted by the secondary channel of the data modem to a distant station. An output from the test set used only with the Dual Data Rate option.
15	114	DB	Transmitted Signal Element Timing (TC)	Signals on this line are used to provide the test set with signal element timing information. An input to the test set. Not used when testing asynchronous modems.
16*	119	SBB	Secondary Received Data (RD)	This lead carries the signals that are generated by the data modem on the secondary channel in response to signals from a distant station. An input to the test set used only with the Dual Data Rate option.
17	115	DD	Receiver Signal Element Timing (RC)	Signals on this line are used to provide the test set with signal element timing information. An input to the test set. Not used when testing asynchronous modems.
18*				Not used.
19*	120	SCA	Secondary Request to Send (RTS)	An "on" condition on this lead indicates that the test set is ready to transmit data on the secondary channel. An output from the test set used only with the Signal Monitoring and Dual Data Rate options.
20	108.2	CD	Data Terminal Ready (DTR)	An "on" condition on this lead indicates that the test set is ready to process data. An output from the test set.

* These leads not normally included in cable supplied with test set, unless unit is equipped with the options specified.

Table 1 (cont.)

21*	110	CG	Signal Quality Detector (SQ)	An "on" condition on this lead indicates that signal quality received by the modem is above a prescribed threshold. An input to the test set used only with the Signal Monitoring option.
22*	125	CE	Ring Indicator.	Not used by test set.
23*	111/112	CH/CI	Data Signal Rate Selector	Not used by test set.
24*	113	DA	Transmitter Signal Element Timing	Signals on this line are used to provide the transmitting modem with signal element timing information. An output from the test set. Available only as an option.
25*				Not used.

*These leads not normally included in cable supplied with test set, unless unit is equipped with the options specified.

The standard Test Set with RS232 interface has a noise immunity of 4 V nominal. The negative threshold is set at -2 V and the positive threshold is set at +2 V. Clamping circuitry allows the positive threshold to be exceeded with signals as large as +25 V and the negative threshold to be exceeded with signals as large as -25 V. See Figure 2 and 3 for threshold and interrelationship details.

6.4.1 Transmitter Data

Output Amplitude: +12 V = Logic "0" = Space; -12 V = Logic "1" = Mark. Output Impedance: 600 ohms.

6.4.2 Transmitter Clock

Input Amplitude: ± 3 V to ± 25 V; Input Impedance: 3000–7000 ohms.

6.4.3 Receiver Data

Input Amplitude: ± 3 V to ± 25 V; Input Impedance: 3000–7000 ohms.

6.4.4 Receiver Clock

Input Amplitude: ± 3 V to ± 25 V; Input Impedance: 3000–7000 ohms.

6.5 MIL 188 Interface

The MIL 188 interface (optionally available) has a noise immunity of 1 V nominal. The thresholds are set at (+) and (-) $\frac{1}{2}$ V. Clamping circuitry provides over-voltage protection.

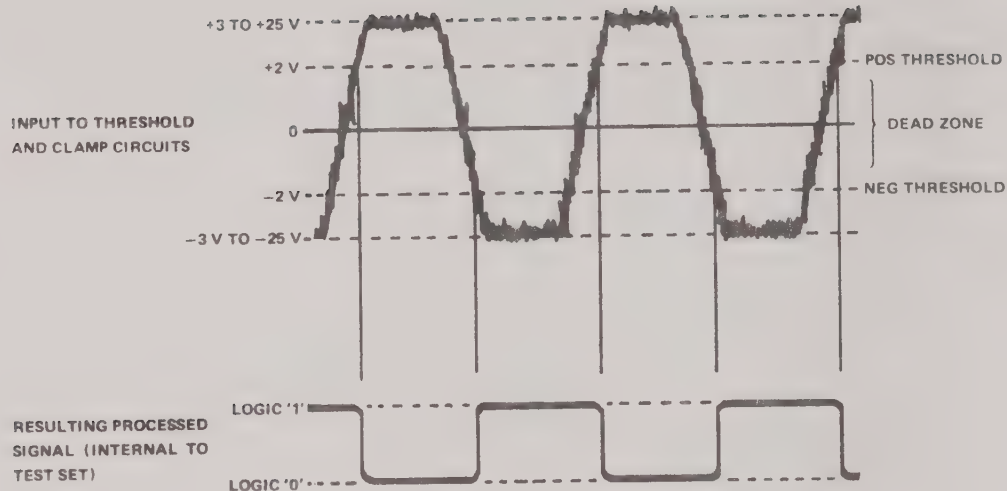
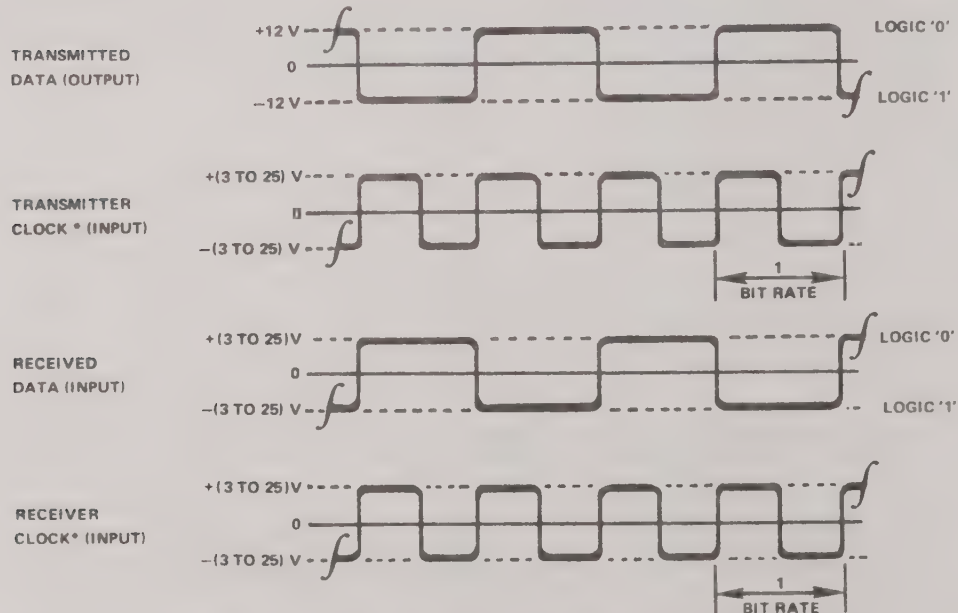


Figure 2. Processing of Input Signals



*CLOCK SIGNALS REQUIRED IN SYNCHRONOUS APPLICATIONS ONLY

Figure 3. Clock/Data Interrelationships

6.6 Special Interface

DTL/TTL and special interface levels are also optionally available.

6.7 Auxiliary Output Connector

An additional output connector labelled Option Connector is located on the rear panel to provide signal required for remote monitoring control, data recording, and more detailed test and analysis. The connector is a Cinch-Jones DB25S. Provides compatibility with the Model 5000 Test Set Printer. All important signals are available at this connector. See Table 2.

Table 2. Option Connector Signals
All output signals are +5 V or 0 V unless otherwise indicated.

Pin No.	Signal	Description
15	1 Unit	BCD Error Counter Readout (0 volts = "One")
14	2 Units	"
12	4 Units	"
13	8 Units	"
10	1 Ten	"
11	2 Tens	"
8	4 Tens	"
9	8 Tens	"
6	1 Hundred	"
7	2 Hundred	"
5	4 Hundred	"
4	8 Hundred	"
17	Reset Error Counter	An external negative pulse resets Error Counter to zero and clears overflow indicator.
24	Receiver in Sync	Signal is 0 volts when receiver is in sync, +5 volts when out of sync.
19	Sync Recovered	Zero level indicates sync has been recovered.
16	Transmitter Clock	Data from modem at transmitter.
22	Receiver Clock	Modem clock if synchronous, recovered clock if asynchronous. For bit sync purposes.
1	Start of Trans Period	Periodic pulse appearing at the beginning of each pseudo-random pattern transmitted.
23	Start of Receiver Period	Periodic pulse appearing in phase with the beginning of each pseudo-random pattern received.
3	Clock Monitor	Positive level indicates clock is present at receiver.
2	Error Pulse	A negative pulse appears each time an error is detected in received sequence.
18	Transmitter Data	Transmitted pseudo-random sequence (± 12 volts).
20	Received Data	Received pseudo-random sequence (± 12 volts).
21	Signal Ground	
25	Chassis Ground	

7.0 OPTIONS

Options are summarized below:

7.1 Carrying Case

A leather carrying case with handle. Space for test set, manual, cords and accessories.

7.2 Rack Mounting

Allows unit to be mounted on a standard rack.

7.3 Dual Data Rate

A double shaft rotary switch allows individual data rates to be selected for the transmitter and receiver sections of the test set. For testing modems with answer-back channels.

7.4 Block Length Selector

Block size selected by front panel rotary switch. Selectable block sizes are: 10^3 , 10^4 , 10^5 , 10^6 , 10^7 , 10^8 bits and 1, 2, 4, 8, 16 and 32 times the word (pattern) length (wl) in bits. A Start Test pushbutton starts the test. A Single/Continuous switch allows analysis of either a single block or repeated blocks. A Test End indicator signals the end of a block during the Single Block test mode.

7.5 Signal Monitoring

A rotary switch and an indicator lamp allows monitoring of six signals in the EIA interface. They are: Data Set Ready, Receive Carrier Detect, Receive Clock, Clear To Send, Transmit Clock and Signal Quality. In addition, toggle switches are provided to control the Request To Send and Data Terminal Ready lines. Secondary channel controls are also monitored and controlled if Dual Data Rate option is also installed.

7.6 Signal Monitoring and Display

Eight individual indicators monitor the following signals in the EIA interface. They are: Receive Data, Receive Clock, Transmit Data, Transmit Clock, Clear To Send, Data Set Ready, Data Carrier Detect, Signal Quality. Also, toggle switches are provided to control the Request To Send and Data Terminal Ready lines. Secondary channel controls are also monitored and controlled if Dual Data Rate option is also installed.

7.7 DTL Signal Interface

All input and output signals are modified to conform to standard DTL signal levels.

7.8 MIL 188 Signal Interface

All input and output signals are modified to conform to MIL 188 standards.

7.9 Divide Data Rate

Allows front panel asynchronous data rate to be divided by a fixed factor, allowing transmitting and receiving at normal speeds in addition to those speeds divided by a fixed factor.

7.10 External Timing Adaptor

Allows receiver section to operate at special data rates in the asynchronous mode. An external clock must be provided to a rear panel BNC connector at 48 times the desired input data rate.

7.11 Y—Connector Cable

Allows testing of two simplex or half duplex modems utilizing a single test set.

7.12 Additional Data Rates

Data rates other than those shown on Data Rate selector rotary switch are provided.

7.13 Current Interface

Allows testing of Bell 300 type modems having a current mode interface. A Burndy-to-EIA cable is provided. Extra cables available.

7.14 Aluminum Carrying Case

A suitcase type carrying case with lock, lined with form-fitted cut sponge.

7.15 3 MHz Operation

This option allows unit to operate synchronously up to 3 MHz.

8.0 APPLICATION

The following is a step-by-step procedure for operating and self-testing a Model 225 Modem Test Set. Figure 4 describes a typical full duplex system to be tested. Referring to Figure 4, the system consists of two pieces of business equipment located at terminals A and B, communicating with one another by means of two full duplex modems and a channel. It is assumed that the modems interface with the business equipment via a standard EIA interface. It can also be assumed that in general the data being transmitted from terminal A to terminal B is completely independent of the data being transmitted in the opposite direction.

8.1 System Test Preparation

The communication system shown in Figure 4 can be tested using two Model 225 Test Sets. In Figure 5, the business equipment at each terminal has been disconnected and a test set substituted. This is accomplished simply by unplugging the EIA standard connectors at the business equipment end and recon-

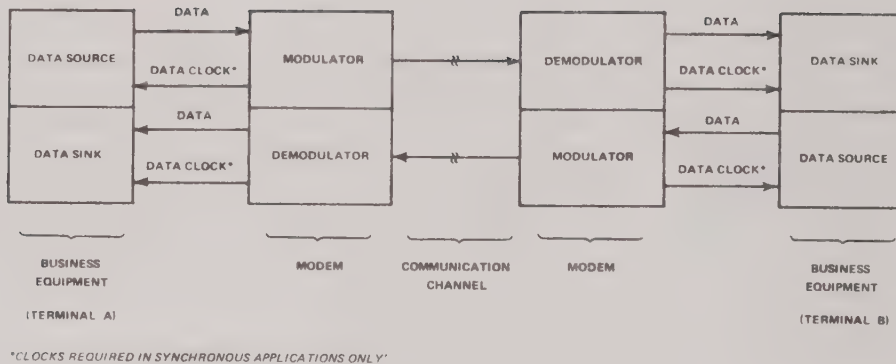


Figure 4. Typical Full Duplex Digital Data Communication System

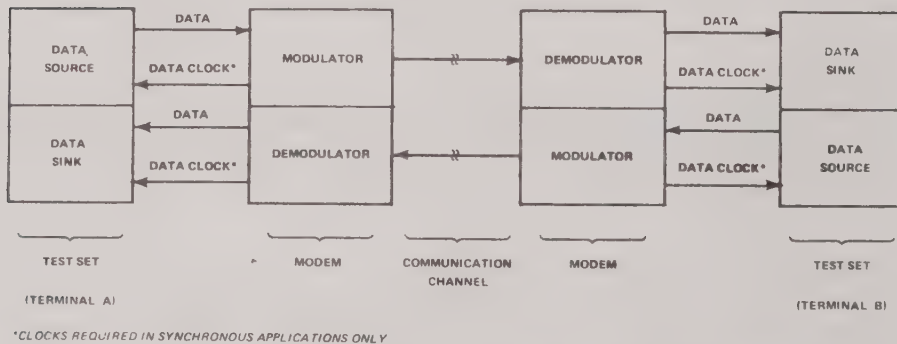


Figure 5. Typical Full Duplex Digital Data Communication System Under Test Using Two Datapulse Test Sets

necting to the Model 225 connector labeled DATA. This will allow the cables from the business equipment to the modem to be tested also. If this is inconvenient, the Model 225 may be connected directly to the modem using the cable supplied with the test set.

8.1.1 Error Detection

The receiver section of each Model 225 generates a pure replica of the pseudo-random patterns generated by the transmitter sections. Upon receipt of a pattern from the modulator sections of their respective modems, the receiver sections synchronize the locally generated pattern with the received pattern and commence a bit-by-bit or block-by-block comparison. A counter is incremented by one each time a bit or block is found to be in error and a digital readout of the cumulative count is displayed on the front panel. When the error count exceeds 999, the overflow indication on the front panel is illuminated and remains on until reset manually. The digital error count and the overflow indicator can be reset by utilizing a pushbutton on the front panel labeled Reset Count.

Thus, bit or block errors that occur due to modem failures or through natural causes in the communication channel while transmitting data from terminal A to terminal B are detected, recorded, and displayed by the test set located at terminal B. The errors occurring during transmission from terminal B to terminal A are detected, recorded, and displayed by the test set located at terminal A. The data patterns used in these tests statistically approximate the data patterns generated by the business equipment.

8.1.2 Lost Synchronization (Synchronous System)

The failure of a synchronous modem to remain in synchronization is detected automatically by the receiver sections of each test set. When the demodulator sections of a modem "slips" a clock period, the received and locally generated pseudo-random data pattern will be displaced by one or more data bits. These two patterns correlate only when exactly synchronized and have zero correlation otherwise. The Model 225 makes use of this statistical property and performs a cross-correlation between the two sequences. Upon detecting 0 correlation, the receiver section resets the error counter to zero, turns off the Sync Locked lamp on the front panel and proceeds to re-establish synchronization. When synchronization has been re-established, the Sync Locked lamp is turned on and, in addition, the Sync Recovered lamp is also turned on. This latter indicator will remain on until manually turned off by the operator. This lamp serves as a memory and indicates to the operator that synchronization has been lost at least once.

8.2 Self-Test

All DATAPULSE test sets may be self-tested, without disconnecting the back panel connectors from the modems. Simply toggle the front panel Test/Operate switch to the test position and utilize the Break Sync and Xmit Errors switches to exercise each test set.

8.2.1 Break Sync Test

Operating the Break Sync pushbutton interrupts the synchronization that was established between the transmitter and receiver sections of the Model 225 Test Set. The Model 225 then exercises its resynchronization circuits to again establish synchronization between the transmitter and receiver sections of the test set. When resynchronization occurs, the Sync Locked and Sync Recovered indicators are illuminated. The Sync Recovered indicator may be extinguished by depressing its reset pushbutton.

8.2.2 Xmit Errors Test

Operating the Force Errors switch initiates the injection of a slow rate error stream into the data flow established between the transmitter and the receiver sections of the Model 225 under test. The errors are detected, accumulated, and displayed as Error Count. If errors in excess of 999 are injected, the Overrange lamp is illuminated. Both the cumulative Error Count and the Overrange indication can be reset by depressing the Reset Count pushbutton.

8.3 Measurement of Bias Distortion

Most of the time a useful communication system operates below the threshold of error. Thus a measurement of errors often gives no information as to how much margin there is against a wrong decision.

It is under these no error conditions that data signal quality measurements are particularly valuable in determining how close to error the system may be. A number of terms describing the quality of binary telegraph signals have been generally accepted. The term distortion is used to mean a change in the received signal from that transmitted. After the received binary signal has been restored to a rectangular shape, distortion takes the form of change in the relative times of the signal transitions. Thus, if the marking and spacing intervals as received differ in duration from those transmitted, they are said to be distorted. A major component of distortion of signal elements is termed bias distortion. Bias distortion is that type which changes sign when the functions of the signaling states are interchanged. For example, a case of bias exists if a marking interval is lengthened in transmission over a system while a spacing interval is shortened. Bias which lengthens marking intervals is termed "marking bias" and is commonly considered as "positive bias". The opposite condition resulting in shortened marking intervals and lengthened spacing intervals is known as "spacing" or "negative bias".

Bias distortion is brought about by a lack of symmetry in the system. For instance, the decision threshold may not be set at the mid-point between the steady-state mark and space conditions, or the shape of the transition from mark to space may differ from that of space to mark.

The amount of distortion is commonly expressed in percent of a unit length signaling element. It then becomes necessary to state the speed of transmission at which the percent distortion applies. Figure 6 gives examples of binary signals having bias distortion.

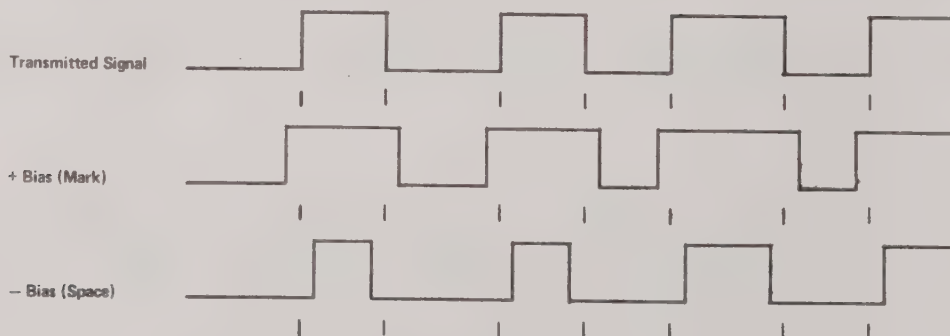
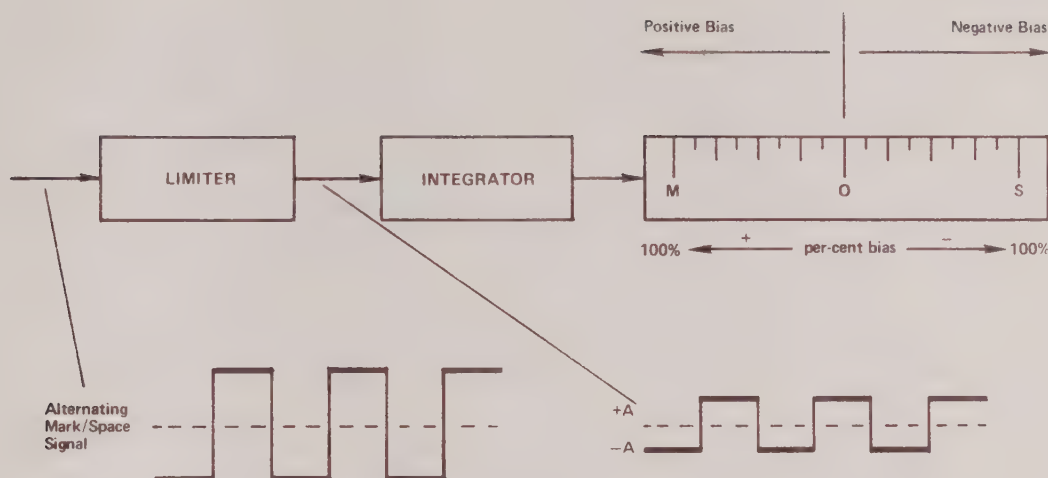


Figure 6. Examples of Bias Distortion

Bias distortion is probably the most common type of data signal distortion. The bias distortion of a transmission link can be readily determined by transmitting a dotting or reversal signal and observing the received signal for equal durations of the mark and space intervals.

The meter deflection is proportional to the average value of the rectangular wave and is, therefore, linearly related to the percentage of the time the signal is in one of its binary states. The meter scale is calibrated to indicate the bias in percent of the unit signal duration. Figure 7 shows the implementation of this measurement technique.

To determine bias distortion of the transmission link or mode, the test set controls are set to transmit a bit stream of alternate marks and spaces (Alt pattern). At the far end of the transmission link, the re-



NOTE: Bias distortion measurements are accurate to within one percent of full scale.

Figure 7. Measurement of Bias Distortion

ceiving test set is used to observe the received signal for equal durations of the mark and space intervals to determine bias distortion.

9.0 WIRING MODEL 225 FOR 115 V, 60 Hz or 230 V, 50 Hz

The Model 225 may be wired to operate from either 115 V, 60 Hz or 230 V, 50 Hz power input. The transformer schematic is shown in Figure 8. The primary terminals are marked 1, 2, 3 and 4.

For 115 V, 60 Hz operation:

- a. Connect terminal 1 to 3.
- b. Connect terminal 2 to 4.
- c. Connect the White power lead that comes from the fuse to terminal 2.
- d. Connect the Blue power lead to terminal 1.

For 230 V, 50 Hz operation:

- a. Connect terminal 2 to 3.
- b. Connect the Blue power lead to terminal 1.
- c. Connect the White power lead that comes from the fuse to terminal 4.

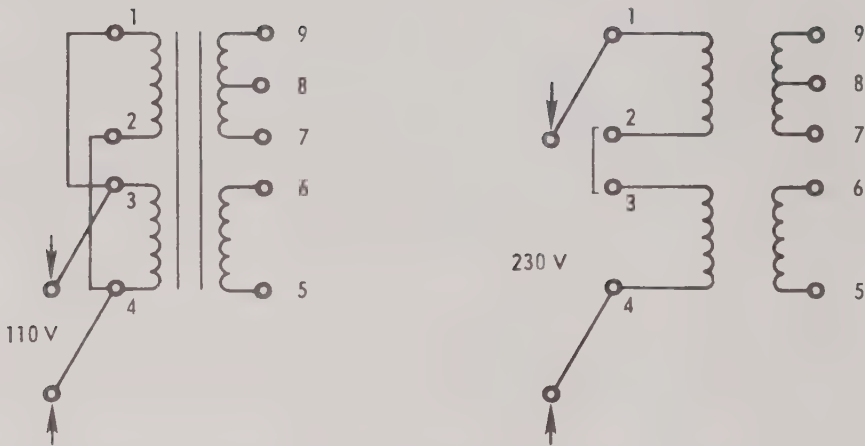


Figure 8. Model 225 Transformer Schematic

The Model 225 is normally wired for 115 V, 60 Hz operation at the factory, and the power socket on the back panel is labeled 115 V, 60 Hz.

For customers wishing to rewire the unit for 230 V, 50 Hz operation, a small tag reading 230 V, 50 Hz is supplied to facilitate relabeling the power socket with the new power constraint. The label adhesive may be activated by brushing on trichlorethylene solvent. An acceptable solvent is manufactured by Metal Craft, Inc., Mason City, Iowa.

10.0 CALIBRATION PROCEDURE FOR MODEL 225 MODEM TEST SET

The following describes a procedure for calibrating the Model 225 Model Test Set. It is assumed that the test set is not connected to any modem during this procedure.

a. SETTINGS

Set Power switch to OFF. Set Invert Data/Normal switch to Normal. Set Receive Only/Transmit Receive switch to Transmit Receive position. Set Xmit Errors switch to OFF. Set Test-Operate switch to Operate. Set Bit Error/Block Error switch to Block Error. Set Pattern switch to pattern length of 2047 bits. Set Data Rate switch to 2400. Turn power ON.

OBSERVATIONS

Bias meter to space condition. Clock Monitor light on. Error count is 000.

b. SETTINGS

Set Test-Operate switch to Test.

OBSERVATIONS

Sync locked light goes on. Bias meter oscillates pseudo-randomly about center position. Note: If NIXIES show errors and the Sync Recovered lamp goes on, depress the Sync Recovered Reset pushbutton.

c. SETTINGS

Xmit Errors switch to ON.

OBSERVATIONS

Error count increases at rate of 1 error per pattern length.

d. SETTINGS

Bit Error/Block Error switch to Block Error.

OBSERVATIONS

Error count increases at rate of 1 error per pattern length.

e. SETTINGS

Xmit Errors switch OFF. Bit Error/Block Error switch to Bit Error. Depress and hold Break Sync pushbutton.

OBSERVATIONS

Clock monitor light goes off.

f. SETTINGS

Release Break Sync pushbutton.

OBSERVATIONS

NIXIES record large number of errors. Overrange lamp lights. Sync Recovered lamp goes on. Error Count resets to 000.

g. SETTINGS

Repeat settings (a) through (f) with Pattern switch set to 511 bit pattern length.

OBSERVATIONS

Identical to observations (a) through (f).

h. SETTINGS

Repeat settings (a) through (f) with Pattern switch set to 63 bit pattern length.

OBSERVATIONS

Identical to observations (a) through (f).

i. SETTINGS

Repeat settings (a) through (f) at each Data Rate.

OBSERVATIONS

Identical to observations (a) through (f).

j. SETTINGS

Pattern switch in Alt position at any data rate except Ext.

OBSERVATIONS

Bias meter oscillates about 0.

k. SETTINGS

Pattern switch in Mark position at any data rate except Ext.

OBSERVATIONS

Bias meter reads M.

l. SETTINGS

Pattern switch in Space position at any data rate except Ext.

OBSERVATIONS

Bias meter reads S.

m. SETTINGS

Repeat steps (a) and (b).

OBSERVATIONS

Repeat steps (a) and (b).

n. SETTINGS

Depress and release Reset Count pushbutton. Allow time for at least one pattern to be analyzed, then depress and hold the Display Block Count pushbutton.

OBSERVATIONS

A three digit number greater than zero is displayed. The Overrange lamp will also be illuminated if 1000 or more patterns have been analyzed.

o. SETTINGS

Release Display Block Count pushbutton.

OBSERVATIONS

Error Count reads 000.

p. SETTINGS

Set Power switch to OFF. Set Invert Data/Normal switch to Normal position. Set Receive Only/Transmit Receive switch to Transmit Receive position. Set Xmit Errors switch to OFF. Set Test-Operate switch to Operate. Set Bit Error/Block Error switch to Bit Error. Set Pattern switch to pattern length of 2047 bits. Set Data Rate switch to External. Apply 2400 b/s square wave to pin 15 and 17 of data connector. Apply Signal Ground to pin 7 of data connector. The MAXIMUM allowable voltage and current excursions for the input square wave are listed below for each interface circuit.

WARNING: DO NOT EXCEED VALUES LISTED!

EIA: -25 V to +25 V.

DTL/TTL: 0 V to 5 V.

MIL 188B: -6 V to 6 V.

CURRENT: 0 mA to 40 mA.

The MINIMUM allowable voltage and current excursions for the input square wave are listed below for each interface circuit.

EIA: -2 V to 2 V.
DTL/TTL: 0 V to 1.2 V.
MIL 188B: -0.6 V to 0.6 V.
CURRENT: 5 mA to 23 mA.

Vary amplitude of input square wave over above ranges specified for interface circuits installed in test set. Connect pin 2 and pin 3 together on back panel of data connector. Turn Power switch ON. Set the Xmit Errors switch to Xmit Errors position.

OBSERVATIONS

Sync locked light goes on. Bias meter oscillates in a pseudo-random manner about the center position. (Note: If NIXIES show errors prior to resetting to 000, the Sync Recovered lamp will go on. Extinguish this lamp by depressing the Sync Recovered Reset pushbutton.) Errors are detected at the rate of 1 error per pattern while Xmit Errors switch is in the Xmit Errors position.

11.0 DETAILED OPTION DESCRIPTIONS

11.1 Data Synchronizing Option

The Model 225 with Data Synchronizing Option allows the receiver section of the Model 225 to operate at asynchronous speeds other than those available by selection on the front panel. A slide switch and four BNC connectors are provided in the back of the unit for this purpose. All interface levels for the BNC connectors are standard DTL/TTL logic. The function of each of the input signals is described below:

- a. DATA IN—This connector allows the input data to drive the receiver portion of the Model 225.
- b. 48 X RATE (REF)—This connector allows the external clock to drive the clock recovery system in the Model 225. The clock does not need to be phased with the data presented at the Data In input but it must be within 2% of the Data In data rate.
- c. DATA OUT—The connector allows the output data of the transmitter portion of the Model 225 to drive external equipment. This data is synchronized with the Clock Out output.
- d. CLOCK OUT—This connector allows the synchronized output clock to clock the Data Out to external equipment.
- e. FRONT PANEL (OTHER)—This is a slide switch which when in Front Panel position allows the Model 225 to operate with its own front panel selected data rates. When in Other position, it operates as a data synchronizing terminal at any data rate dictated by the Data In and 48 X Rate Reference clock.

11.2 Signal Monitoring Option

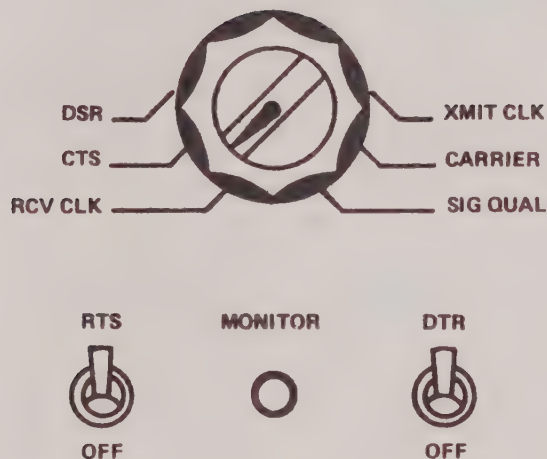


Figure 9. Signal Monitor Option

The purpose of this option is to allow certain key signals at the EIA interface to be controlled and monitored. A six-position rotary switch mounted on a concentric shaft along with the pattern selection switch, allows the selection and monitoring of any one of six lines. In addition, two toggle switches allow control of the Request To Send and Data Terminal Ready lines. These lines and their associated EIA pin assignments are given in Table 3.

Table 3

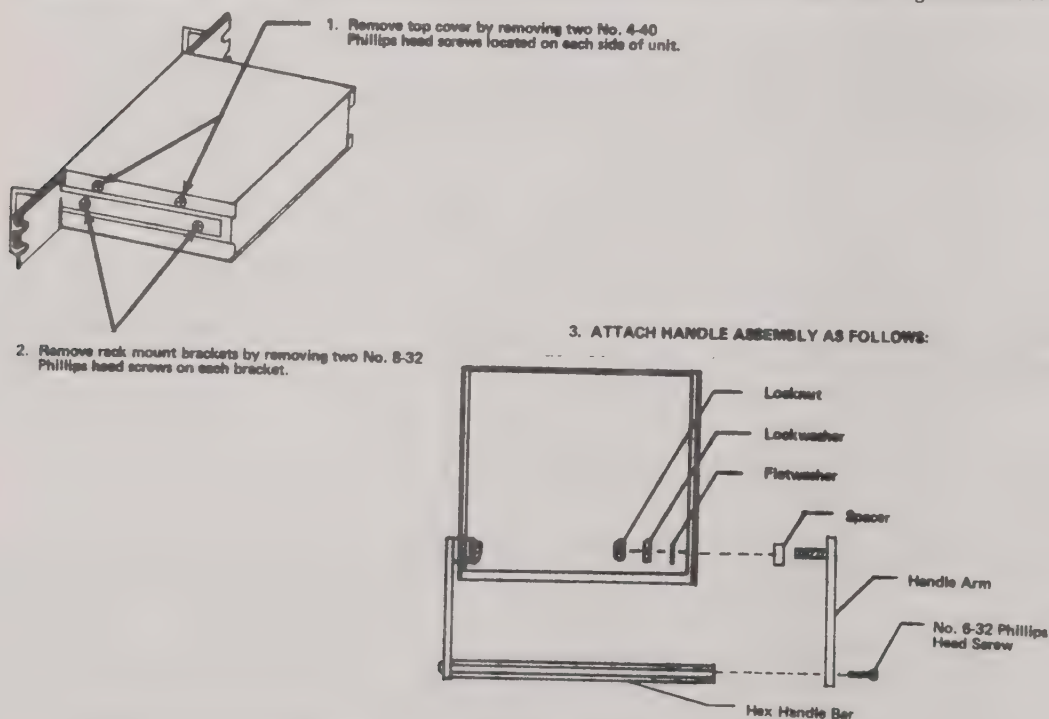
Data Connector Pin Number	RS232B or C Designation	Front Panel Label	Description
6	CC	DSR	Data Set Ready
5	CB	CTS	Clear To Send
17	DD	RCV CLK	Receiver Signal Element Timing
15	DB	XMT CLK	Transmitted Signal Element Timing
8	CF	CARRIER	Receive Line Signal (Data Carrier) Detector
21	CG	SIG QUAL	Signal Quality Detector
4	CA	RTS	Request To Send
20	CD	DTR	Data Terminal Ready

In order to monitor the status of any of the above signals, select the desired signal with the topmost (red) knob on the Monitor rotary switch. If the status of the selected line is "on", then the Monitor light directly beneath the Monitor rotary switch will be illuminated. Conversely, the light will remain extinguished for all "off" conditions.

Note that the Received Data line (pin 3, RS232B or C designation "BB") is continually monitored by the test set bias meter. The Transmitted Data (pin 2, RS232B or C designation "BA") is not monitored but can easily be checked by putting the test set into the Test condition, thus tying the Transmitted Data into the Received Data, and observing the bias meter.

11.3 Rack Mounting Option

Instructions for converting a rack mount to a table top model with handle are given below:



- At threaded standoff end of handle arm, add one spacer.
- Insert this end into chassis.
- Fasten flatwasher, lockwasher and locknut to standoff. NOTE: Do not tighten locknut completely at this time.
- Repeat above procedure for other handle arm.

- e. Locate hex handle bar between arms and fasten with No. 6—32 Phillips head screw.
- f. Tighten two locknuts located inside chassis at this time. IMPORTANT: Do not over tighten or handle arm will not move freely.

11.4 Increased Operating Speed Option

The Model 225 Modem Test Set can be optionally conditioned to operate at synchronous data rates of up to 3 MHz typical, 4 MHz maximum. The signals are made available at the rear panel utilizing four BNC connectors as shown in Figure 10.

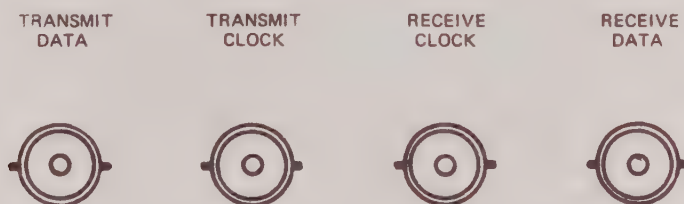


Figure 10. High Frequency Signals at Rear Panel BNC Connectors

Transmit Data is an output signal. Receive Data, Receive Clock and Transmit Clock are input signals. All signals are DTL/TTL levels, 0 V to +5 V nominal. When the BNC inputs and outputs are being used, the EIA connector labeled Data must be open. When the EIA connector inputs and outputs are being used, the BNC connectors must be open.

12.0 MODEL 225—S30453 MODEM TEST SET

The Model 225—S30453 Modem Test Set is basically a standard Model 225 Modem Test Set with some additional special features. In addition to the normal patterns, the operator is allowed to select three additional repeating patterns, i.e., a 240-bit pattern made up of a 7-bit, manually selected preamble followed by 233-bits of pseudo-random data; a 600-bit pattern made up of a 13-bit preamble followed by 587-bits of pseudo-random data; and a 1200-bit pattern made up of a 24-bit preamble followed by 1176-bits of pseudo-random data. All preambles are selected via 24 front panel switches. A bit error analysis is performed on the entire pattern including the manually selected portion, thus both transmitted and receiver preambles must be identical. All of the other operations of the test set function in the normal manner.

13.0 SPECIAL SWITCHES AND CONNECTORS

13.1 Pattern

Three additional positions for selection of the three special preamble sequences are provided on the front panel Pattern switch. These positions are labelled 7/240, 13/600 and 24/1200 and select, respectively,

the 240-bit sequence which includes the 7-bit preamble, the 600-bit sequence which includes the 13-bit preamble, and the 1200-bit sequence which includes the 24-bit preamble.

13.2 Preamble

Twenty-four two position toggle switches mounted on the front panel. The switches are labelled 1 through 24 starting with the Least Significant Bit (LSB) and ending with the Most Significant Bit (MSB). In all cases, bit 1 or the LSB is transmitted first followed by the rest of the preamble. The size of the preamble is selected by the Pattern switch.

13.3 Block Analyzed Pushbutton

A two position toggle switch located on the rear panel of the test set with positions labelled Normal Operation and Delete Pause. This toggle switch controls the operation of the pushbutton labelled Blocks Analyzed located on the front panel of the test set. In the Normal position, the front panel Blocks Analyzed pushbutton functions normally, i.e., the analysis is paused while the pushbutton is depressed. In the Delete Pause position, the bit error analysis continues while the front panel Blocks Analyzed pushbutton is depressed.

13.4 Timing Outputs

A 25-pin connector located on the back panel. The signals which appear on this connector are listed below:

<u>Pin</u>	<u>Signal</u>
1	Frame Ground
2	300 b/s Transmitter Clock
3	600 b/s Transmitter Clock
4	1200 b/s Transmitter Clock
5	1800 b/s Transmitter Clock
6	2000 b/s Transmitter Clock
7	Signal Ground
8	2400 b/s Transmitter Clock
9	3600 b/s Transmitter Clock
10	4800 b/s Transmitter Clock
11	7200 b/s Transmitter Clock
12	9600 b/s Transmitter Clock
13	10,800 b/s Transmitter Clock
14	Ext Transmitter Clock
15	Transmitted Pattern Word Sync
16	Receiver Reference Pattern Word Sync
17-25	Not Used

14.0 THEORY OF OPERATION

To test a modem or a digital communication system for proper operation, we want a test set which will produce digital data to be used as an input to the modem or system and which will be able to look at the output of the modem or system and decide whether the digital information coming out is the same as that which was put in. Further, if the modem or system being tested is causing errors in the data, we want our test set to be able to tell us how many. And, finally, we want our test set to tell us that the modem or system can handle any data pattern that it might possibly see, not just one, two, or three particular patterns.

Why do we use PR? Let us back up for a moment and ask ourselves what would be the best way to test a transmitter/transmission path/receiver system which is supposed to operate over a given band of frequencies and a given range of amplitudes. The answer, of course, would be to test it with "white noise". White noise, by definition, contains at random times ALL amplitudes within a given range. If we could prove that our system could handle ALL frequencies and ALL amplitudes within its specifications, we would be certain that it is capable of proper operation at ANY frequency and ANY amplitude within its specifications.

Here, however, we want to do digital testing rather than analog testing. So, we might say if we used "digital white noise" all of the remarks above would apply to testing our digital system. Digital white noise, by definition, would contain all possible data patterns and any pattern would, unfortunately, occur at a completely random time. I say "unfortunately" because therein lies the problem. If a given pattern occurred at a random time, we could never know exactly when it was going to occur and therefore it would be extremely difficult to tell if the system handled it without error.

So, we turn our attention from a random data pattern to the next best thing. A PSEUDO-RANDOM data pattern. What are the differences? In a random data pattern we would see every possible combination of "n" bits. In a PR pattern, we will see every possible combination of "n" bits except one. Therefore, we can say that for "n" bits, PR is almost as good as random. And, as "n" increases, PR gets closer and closer to becoming statistically equal to random. Secondly, and here is the clincher that sways us into using PR rather than random, the sequence of data patterns in a PR word is exactly, mathematically predictable and therefore is exactly repeatable.

It suddenly becomes clear that if we can generate an ALMOST random digital sequence to put into a system to be tested and then we can generate that exact same ALMOST random digital sequence to compare with the output of the system being tested, we can quite easily tell if the system being tested caused any errors in the data. AND THAT IS EXACTLY WHAT WE SAID WE WANTED OUR MODEM TEST SET TO DO.

- a. We can generate a digital sequence which has a whole lot of different data patterns in it.
- b. We can put this sequence into the input of the system we wish to test.
- c. We can look at the output of the system being tested and tell whether it caused any errors in the data that was put into it.

We have said that PR data is easy to generate and that in a PR sequence we will see all but one of the possible patterns of "n" bits that we would expect to see in a comparable random sequence. Let us try to prove these statements through the following examples.

Two basic digital circuits form the heart of a PR generator; a shift register and an exclusive OR (sometimes called a mod 2 adder).

14.1 Shift Register

A basic shift register is composed of two or more flip-flops. Each flip-flop is capable of storing a single bit of data. Therefore, the number of flip-flops in the register determines the number of bits it can store. Figure 11 below is a simplified logic diagram for a basic three-stage shift register.

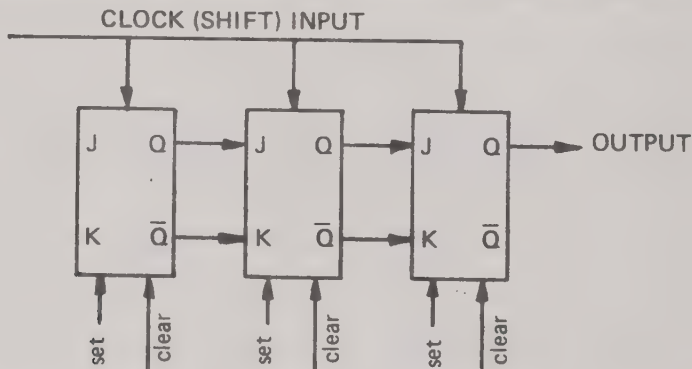
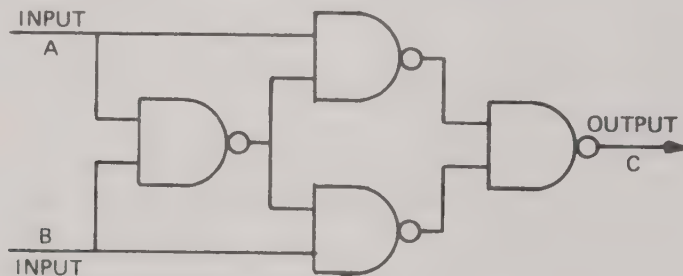


Figure 11. Basic Three-Stage Shift Register

If through the set and clear inputs, we place each flip-flop in a specific state, they will retain this data until a clock pulse is applied. At the time a clock pulse is applied, the data stored in each stage will shift one position to the right. This shift reoccurs each time a clock pulse is applied until the data stored in each of the flip-flops has appeared at the output in serial word format.

14.2 Exclusive OR

An exclusive OR circuit receives data at two inputs and produces one output. Figure 12 shows the logic diagram and truth table for an exclusive OR circuit.



INPUTS		OUT- PUT
A	B	C
1	1	0
0	0	0
1	0	1
0	1	1

Figure 12. Exclusive OR Circuit and Truth Table

From the truth table we see that if the two inputs are the same (both 1's or both 0's), the output will be a 0. If the inputs are different (a 0 and a 1 or a 1 and a 0), the output will be a 1.

Now, let us connect a basic shift register and an exclusive OR circuit as shown in Figure 13 and see what happens.

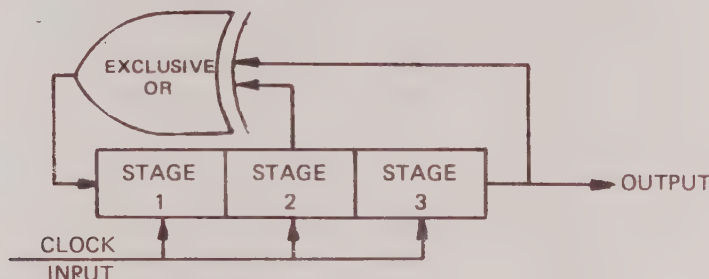


Figure 13. Three-Stage PR Generator

Let us start with stages 1, 2 and 3 having a 1, a 0 and a 0 stored in them, respectively. As we apply successive clock pulses, the following will occur simultaneously. The data stored in stages 2 and 3 are exclusively OR'd to produce an input to stage 1. The data stored in stage 1 is shifted to stage 2, that stored in stage 2 is shifted to stage 3 and that stored in stage 3 is shifted out the output. Figure 14 shows the sequence of data in each stage of the three-stage shift register. Note that the data in each stage is exactly identical to that in each other stage but is delayed one bit time in successive stages. We see that the output (in this example taken from stage 3) is a repetitive 7-bit PR block or word.

Now let us examine the 7-bit PR word we have generated and satisfy ourselves that it does indeed contain all of the possible patterns of "n" bits except one. In our example we are using a three-stage shift register which we said is capable of storing 3 bits of information at one time. Therefore, we expect our PR sequence to contain all possible combinations of 3 bits except one. Let us examine it.

The word we generated repetitively was "0 0 1 0 1 1 1". Using this word and a table showing all of the possible combinations of 3 bits, Figure 15 shows that the sequence does contain all of the possible combinations except one.

The only possible combination of 3 bits that does not occur in a PR sequence generated by a three-stage shift register is three consecutive 0's. Every other possible combination occurs once and only once in each block of the sequence.

We can show by the same analysis that a four-stage shift register will produce a repetitive PR sequence of 15 bits per block which contains all of the 16 possible combinations of 4 bits except 4 consecutive 0's; a five-stage register, 31 bits per block with all of 32 combinations except 5 consecutive 0's, etc., etc.

In general, an "n" stage shift register with exclusive OR feedback will produce a maximal length repetitive PR sequence, $2^n - 1$ bits in length, which contains all of the 2^n possible combinations of "n" bits except "n" consecutive 0's.

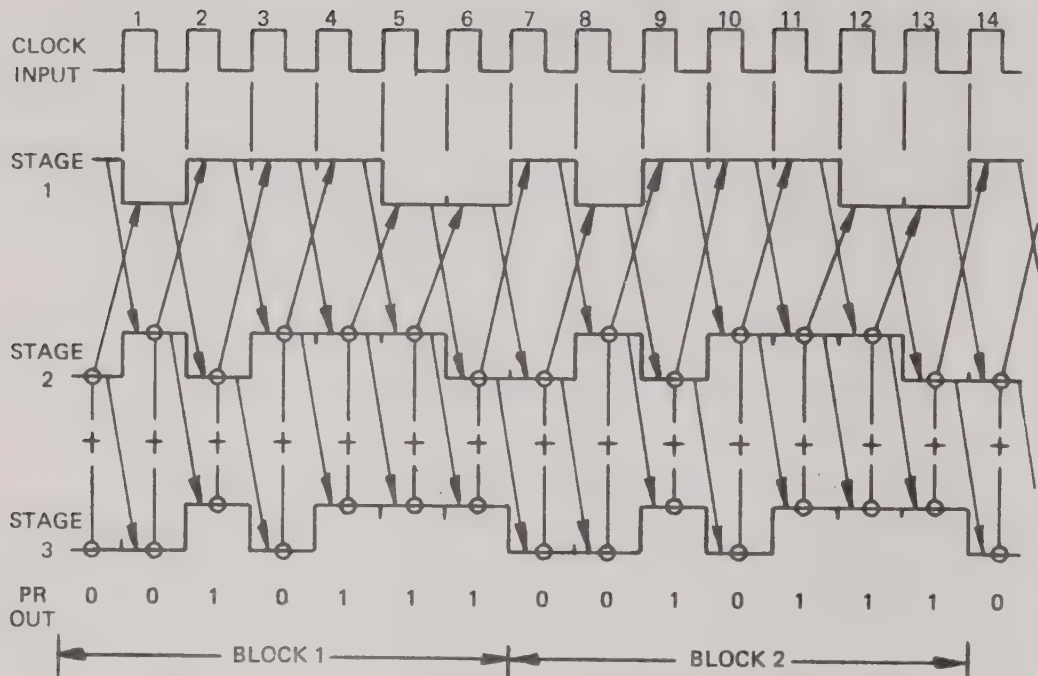


Figure 14. PR Word Generation using a Three-Stage Shift Register

We have seen how PR data sequences are generated and have reviewed some of its properties. We now have the necessary background to study how these techniques are used in the DATAPULSE line of modem test equipment.

14.3 The Transmitter Section

The transmitter section of your modem test set contains the shift register and exclusive OR circuit to generate a PR sequence to be used in testing modems or digital communication systems. In addition, it also contains the circuitry for supplying clock or shift pulses to the shift register and output buffer circuitry for presenting the PR data at the output in the proper format.

All of the DATAPULSE test sets utilize an eleven stage shift register which is capable of repetitively producing a PR word or block which is $2^{11}-1$ or 2047 bits in length and contains all 2048 possible combinations of 11 bits except eleven consecutive 0's. A simplified block diagram of the transmitter section is shown in Figure 16.

Note that this is exactly the same circuit as that which we studied in Figure 13, except that this shift register contains 11 stages for producing 2047 bit words. Note that the feedback points are stages 11 and 9. These are determined mathematically to be the proper feedback stages to produce the maximal length (2047 bit) word.

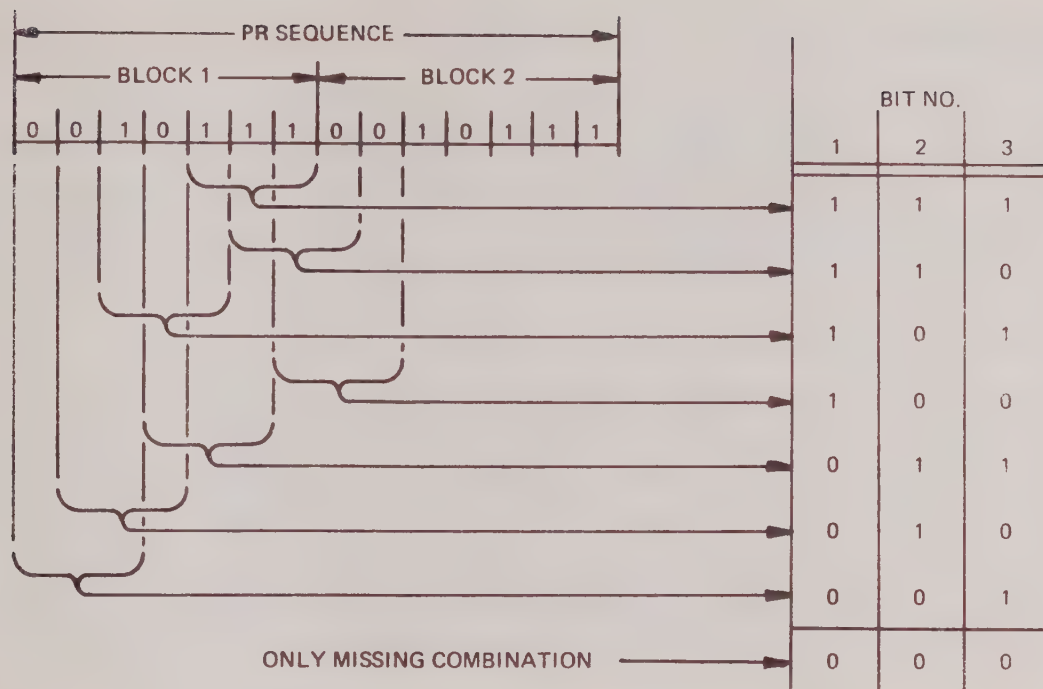


Figure 15. Bit Combinations in a PR Sequence

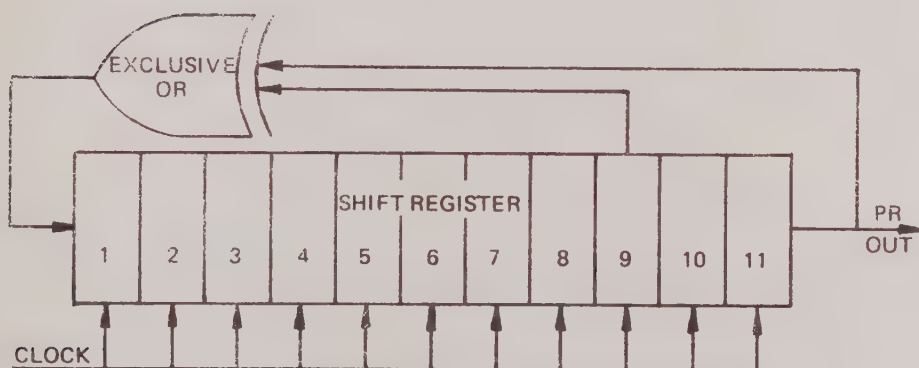


Figure 16. PR Generation, Transmitter Section

14.4 The Receiver Section

The receiver section of your modem test set contains a shift register/exclusive OR PR generator that is identical to that found in the transmitter section. In addition, it contains circuitry for synchronizing the data generated in this second generator with the data being received from the system under test. It contains clock correction circuitry to insure that the clock used in the receiver PR generator is synchronized with that of the received data. It contains error detection circuitry. It contains circuitry to count and display bit or block errors and total blocks generated. And, finally, it contains circuitry for measurement and adjustment of bias distortion. Let us study these important features of the receiver section.

14.5 PR Regeneration and Error Detection

In the transmitter section described in paragraph 14.3, we generated a repetitive 2047 PR data pattern to be transmitted into a system to be tested. That pattern is put through the system being tested and is taken from that system's output into the input of the receiver section of the test set. At this point we will generate a second 2047 bit PR data pattern which is identical to the one we produced in the transmitter section. We will then compare the data from this second generator with the data which has come through the system being tested. If there are differences in the two data streams, we will know that the system under test has caused errors in the first data stream we generated. Figure 17 is a block diagram of the receiver section PR generator and error detection circuits. Note that when the Data Sync switch is in position A, the incoming data will be loaded directly into the eleven-stage shift register. When the switch is in position B, the input to the shift register is disconnected from the incoming data and connected to the output of the exclusive OR feedback.

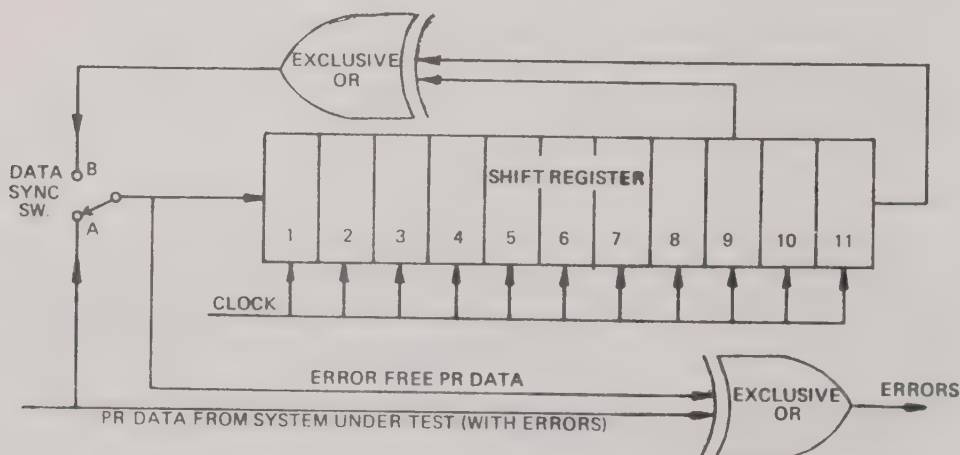


Figure 17. Receiver Section, PR Generation and Error Detection

Let us study what happens when a data stream arrives from a system under test. The Data Sync switch is in position A. Let us call the first bit in the data stream Bit A (note that this was the first bit out of the transmitter PR generator), the second bit Bit B, the third Bit C, the eleventh Bit K, the twelfth Bit

L, etc. Bits A through K will step into the register with the first 11 clock pulses. Let us stop the action here and examine what we have.

Bit A is in stage 11 of the receiver PR generator, Bit B in stage 10, Bit K in stage 1. The receiver PR generator now contains the identical eleven bits that were stored in the transmitter PR generator when it started sending a signal through the system being tested. The next bit that the transmitter sent was Bit L. If, at the time Bit A arrives in receiver shift register stage 11 (Bit K in stage 1), we electronically throw the Data Sync switch to position B, the receiver shift register will start generating a PR data stream identical to that generated by the transmitter. The next bit into stage 1 will be Bit L. This is the same as the Bit L that is coming into the receiver from the system under test. **THE RECEIVER PR GENERATOR IS SYNCHRONIZED TO THE INCOMING DATA.** The incoming data (if there are no errors in it) will be identical to the data being generated in the receiver PR generator at the input to stage 1 of the shift register.

Now, let us look at error detection. We learned earlier that if the two inputs to an exclusive OR circuit are the same (00 or 11), the output will be 0. If they are different (01 or 10), the output will be 1. Look again at Figure 17. When the Data Sync switch was in position A, the error detecting exclusive OR circuit was receiving the incoming data at both of its inputs simultaneously. The output of it had to be 0. After switching to position B, one of its inputs is the PR data being generated in the receiver PR generator. The other input is still the incoming data. As long as there are no errors in the incoming data, the output of the error detecting exclusive OR will be 0. If, however, the system under test has caused an error in the incoming data, the data streams, at the time of the error, will be different and the output of the exclusive OR will be 1.

We now have an instrument which:

- a. Generates a PR data stream and transmits it through a system under test.
- b. Synchronizes to the data stream coming from the system under test and generates a second, identical PR data stream.
- c. An exclusive OR which compares the two and produces a 1 output each time there is an error in the data coming from the system being tested.

14.6 Synchronization

We saw how the modem test set receiver synchronizes to the incoming data by shifting the first 11 bits of incoming data into its shift register, at which time it automatically switches to a PR generator configuration and generates a PR data stream which is started with that particular 11 bits.

Suppose though, that the system under test had caused one or more errors in the first incoming eleven bits. The receiver PR generator would then be synchronized to a false pattern and the transmitter and receiver PR generators would not really be synchronized. Many false errors would be produced from the error detecting exclusive OR. In other words, the error rate would be extremely high.

Built into the DATAPULSE Modem Test Set receivers is circuitry which constantly monitors the error output. If it detects error rates above a certain preset figure, it automatically switches the Data Sync

switch back to position A and goes through the entire synchronization cycle again. It will continue to do this automatically until it does synchronize on valid data.

14.7 Clock Correction

When testing synchronous modems or synchronous systems, a clock which is synchronized with the data is supplied by the modem to the test set receiver. When testing asynchronous systems however, a clock for the test set receiver section must be generated within the test set. Basically, the clock for both the transmitter and receiver portions of the DATAPULSE test sets are derived from a crystal controlled oscillator divided down to the desired data rate. What though if there are delays through the system being tested that vary from time to time, having the effect of varying the clock time of the transmitted data with respect to the clock time of the receiver generated data. This would have the effect of de-synchronizing the two data streams and errors would be sensed even though there might not be any in the incoming data.

In order to eliminate this possibility, DATAPULSE Modem Test Sets contain circuitry which automatically and continuously corrects the receiver clock frequency so that the receiver clocks are always very nearly coincident in time with transition times of the incoming data. Figure 18 is a simplified block and timing diagram of this clock correction circuit.

A basic frequency is selected in the receiver which is 32 times the frequency of the basic data rate being used in the transmitter. This signal is put through a "Add/Delete a Pulse" circuit and is then divided by 32 to form the clock to be used in the receiver. If there was no instruction to add or delete a pulse, the frequency of the receiver clock is the same as that of the transmitter clock and the transitions of the incoming data coincide with the clock times of the receiver.

If however, for any reason the transition time of an incoming data bit occurs prior to the positive-going edge of a receiver clock, the Zero Crossing Comparator will detect this and will add one pulse to the 32 times data rate stream. When this stream is subsequently divided by 32, the corrected clock output will occur slightly sooner than normal and the receiver clock will be corrected in the proper direction to make it coincide with the incoming data transition times. If, on the other hand the clock starts to occur before the data transition time, a pulse will be deleted from the 32 times data rate stream and the corrected clock will be corrected in the opposite direction.

The clock correction circuitry will continuously make comparisons with each transition of the incoming data and correct the receiver clock so that it is timed coincident with the incoming data.

14.8 Bit/Block Error Count and Display

The receiver portion of each DATAPULSE Modem Test Set contains counter circuitry for counting either each bit that is in error or each block which contains one or more errors. On some models only bit errors may be counted. On others bit or block error count may be selected by front panel switch.

The output of this counter is continuously displayed on a three-digit nixie display at the instrument front panel. A front panel overrange indicator lights when the count on the error indicator passes through a count of 999. Thus, a total error count of 1999 may be displayed without resetting the counter.

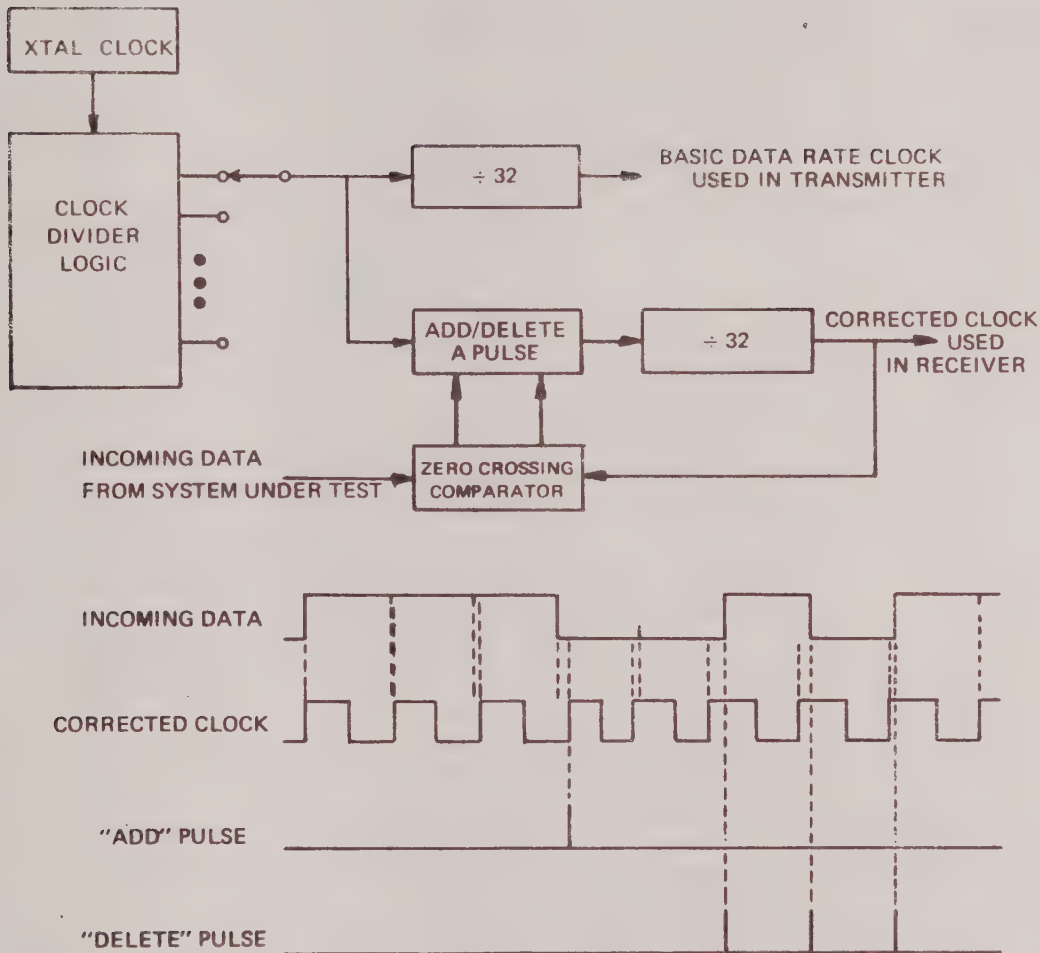


Figure 18. Block and Timing Diagram, Clock Correction Circuit

14.9 Block Count

One modem test set contains a second counter which continuously counts blocks of data received regardless of errors. This counter may be displayed on the bit/block error display by actuation of a front panel pushbutton.

MODEL 225
S30453

15.0 PARTS LIST

15.1 A 1 Board

REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
A1	1		SW	SN9601N
A2	3		Motorola	MC858P
A4	9		Motorola	MC857P
A5	3		Motorola	MC1807P
A6	2		Motorola	MC856P
A7		Same as A4		
A8		Same as A2		
A9		Same as A5		
A10	4		Motorola	MC849P
A11		Same as A10		
A12	4		Motorola	MC845P
A13	1		Motorola	MC863P
A14	11		Motorola	MC855P
A15		Same as A14		
A16	2		Motorola	MC1801P
A17	2		Motorola	MC1805P
A18	10		Motorola	MC1809P
A18A		Same as A4		
A19		Same as A4		
A20		Same as A4		
A21		Same as A4		
A22	1		Motorola	MC3062P
A23		Same as A14		
A24		Same as A14		
A25		Same as A14		
A26		Same as A14		
A27		Same as A12		
A27A		Same as A12		
A28	9		TI	SN7490N
A29		Same as A28		
A30		Same as A28		
A31		Same as A28		
A32		Same as A28		
A33		Same as A28		
A34		Same as A5		
A35		Same as A4		
A36	2		TI/National	SN7486P
A36A		Same as A18		

REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
A37		Same as A18		
A38		Same as A18		
A39		Same as A18		
A40		Same as A18		
A41		Same as A18		
A42		Same as A18		
A43		Same as A6		
A44		Same as A2		
A45		Same as A10		
A46		Same as A4		
A47	3		TI	SN74141N
A48		Same as A47		
A49		Same as A47		
A50		Same as A12		
A51		Same as A14		
A52		Same as A14		
A53		Same as A14		
A54		Same as A14		
A55		Same as A14		
A56		Same as A10		
A57		Same as A16		
A58		Same as A17		
A59		Same as A18		
A60		Same as A36		
A61		Same as A18		
A62		Same as A4		
A63		Same as A28		
A64		Same as A28		
A65		Same as A28		
C1	1	12 μ F, 350 V, Electrolytic	Cornell Dubilier	WBR 12-350
C2	2	22 μ F, 20 V, Tant.	Sprague	CS13BD226K
C9	1	500 μ F, 16 V, Electrolytic	Cornell Dubilier	WBR 500-16
C10		Same as C2		
C11	3	0.014 F	Kemit	CK05BX103K
C12		Same as C11		
C13		Same as C11		
CR1	1		Motorola	1N4006
CR5	1		Motorola	2N5060
Q1	1		Motorola	2N4851
R1	1	100 k, $\frac{1}{2}$ W		RC20GF104J
R2	1	8.2 k, $\frac{1}{2}$ W		RC20GF822J
R3	1	620 ohm, $\frac{1}{2}$ W		RC20GF621J
R4	1	10 ohm, $\frac{1}{2}$ W		RC20GF100J

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REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
R5	1	200 ohm, ½ W		RC20GF201J
R6A	4	2 k, ½ W		RC20GF202J
R7	1	5 k, ½ W	Bourns	3339H-1-502
R8		Same as R6A		
R9	4	1 k, ½ W		RC20GF102J
R10	1	18 k, ½ W		RC20GF183J
R11		Same as R6A		
R13	3	33 k, ½ W		RC20GF333J
R14		Same as R13		
R15		Same as R13		
R16		Same as R9		
R19		Same as R6A		
R20		Same as R9		
R21		Same as R9		
V1	3		Burrough	B5440
V2		Same as V1		
V3		Same as V1		
XA1	1		Augat	314-AG5D-2R
XA2	3		Augat	326-AG5D-2R
XA3		Same as XA2		
XA4		Same as XA2		
XV1	3		Burrough	SK196
XV2		Same as XV1		
XV3		Same as XV1		
15.2	<u>A 2 Board</u>			
A1	1		Beckman	898-3-R220
A2	4		Motorola	MC1807P
A3	10		Motorola	MC849P
A4	1			CM1150
A5		Same as A3		
A6		Same as A3		
A7		Same as A3		
A8		Same as A3		
A9	3		Motorola	MC837P
A10		Same as A9		
A11	2		Motorola	MC1809P
A12		Same as A2		
A13	1		Cermetec	CM1162/MC1489L
A14		Same as A2		
A15	4			SW9601
A16		Same as A15		

REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
A17		Same as A15		
A18		Same as A15		
A19		Same as A3		
A20	2		Cermetec	CM1160/N8T16A
A21		Same as A20		
A22		Same as A11		
A23	5		TI	SN7493N
A24	7		Motorola	MC855P
A25		Same as A23		
A26	6		Motorola	MC853P
A27	1		Motorola	MC1801P
A28		Same as A24		
A29		Same as A24		
A30	1		Cermetec	CM1151/MC1488L
A31		Same as A9		
A32		Same as A3		
A33		Same as A24		
A34		Same as A24		
A35		Same as A3		
A36		Same as A26		
A37	7		TI	SN7490N
A38		Same as A37		
A39		Same as A37		
A40		Same as A3		
A41	1		Motorola	SN7486N
A42	3		Motorola	MC858P
A43		Same as A37		
A44		Same as A37		
A45		Same as A26		
A46		Same as A2		
A47		Same as A26		
A48	1		TI	SN74L00N/SN7400N
A49		Same as A24		
A50		Same as A23		
A51		Same as A42		
A52	1		Beckman	899-1-R330
A53		Same as A37		
A54		Same as A37		
A55		Same as A26		
A56		Same as A26		
A57		Same as A3		
A58		Same as A24		

MODEL 225
S30453

REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
A59		Same as A42		
A60		Same as A23		
A61		Same as A23		
C1	7	0.01 μ F		CK05BX103K
C2	9	0.001 μ F		CK05BX102K
C3		Same as C2		
C4		Same as C2		
C5		Same as C2		
C6		Same as C2		
C7		Same as C2		
C8	5	22 mF, 15 V		C513BD226K
C9		Same as C8		
C10		Same as C8		
C11		Same as C8		
C12		Same as C2		
C13		Same as C2		
C14		Same as C2		
C15		Same as C1		
C16		Same as C1		
C17		Same as C1		
C18		Same as C1		
C19		Same as C1		
C20		Same as C8		
C21		Same as C1		
C22	2	0.1 μ F		CK06BX104K
C23		Same as C22		
R1	4	18 K		RC20GF183J
R2		Same as R1		
R3		Same as R1		
R4		Same as R1		
R5	2	510 ohm		RC20GF511J
R6	2	1 K, 1/4 W		RC07GF102J
R7		Same as R5		
R8		Same as R6		
XA1	4		Augat	314-AG5D-22
XA2		Same as XA1		
XA3		Same as XA1		
XA4		Same as XA1		
P1	1		Elco	6007-044-980-002
Y1	1	7648 MHz, $\pm 0.005\%$	CTS Knight	

15.3 A 3 Board

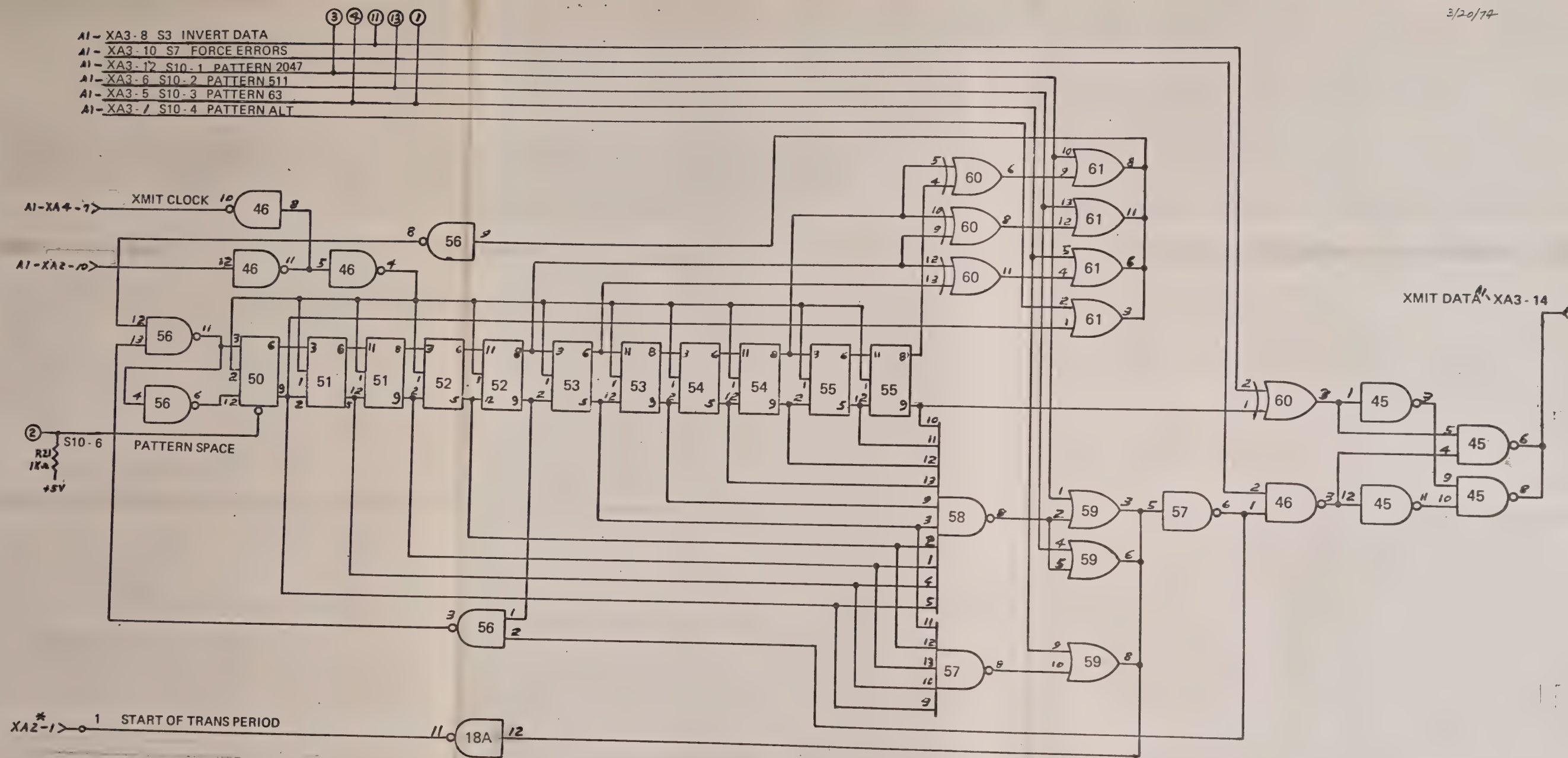
REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
A1	8		TI	7495
A2		Same as A1		
A3		Same as A1		
A4	2		TI	7430
A5	2		TI	7420
A6		Same as A1		
A7	4		TI	7404
A8	2		TI	7400
A9	1		TI	7402
A10	5			2P14R
A11	2		TI	7486
A12		Same as A7		
A13	2		Motorola	MC849
A14	4			CM1152/1488
A15		Same as A10		
A16		Same as A14		
A17		Same as A14		
A18		Same as A14		
A19	4		TI	7492
A20	5		TI	7493
A21		Same as A20		
A22		Same as A20		
A23		Same as A20		
A24		Same as A19		
A26		Same as A19		
A27		Same as A19		
A28	5		TI	74107
A29		Same as A28		
A30		Same as A8		
A31	6		TI	74165
A32		Same as A31		
A33		Same as A31		
B1		Same as A1		
B2		Same as A1		
B3		Same as A1		
B4		Same as A4		
B5		Same as A10		
B6		Same as A1		
B7		Same as A7		
B8		Same as A20		

MODEL 225
S30453

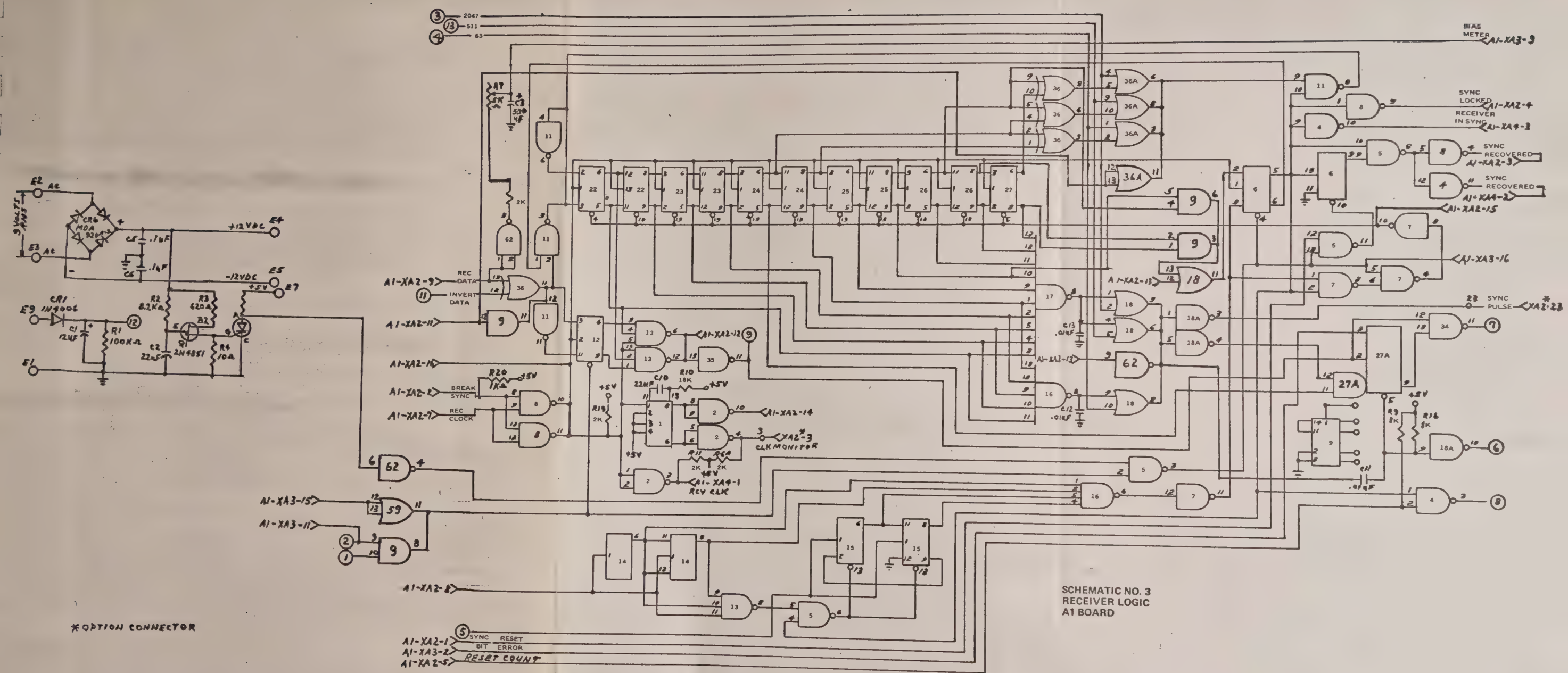
REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
B9	1		TI	7451
B10		Same as A28		
B11		Same as A28		
B12	4		TI	7474
B13		Same as A28		
B14		Same as A28		
B15		Same as B12		
B16		Same as A10		
B17		Same as A13		
B18		Same as B12		
B19	1		TI	7432
B20		Same as A5		
B21		Same as A10		
B25		Same as A11		
B30		Same as B12		
B31		Same as A31		
B32		Same as A31		
B33		Same as A31		
C1	2	0.01 μ F		CK05BX103K
C2	1	22 μ F, 15 V		C513BD226K
C3		Same as C1		
R1	2	1 k, $\frac{1}{2}$ W		RC20GF102J
R2		Same as R1		
Y1		2.592 MHz		

15.4 Front Panel Controls

REF. NO.	QTY. USED	DESCRIPTION	MFR.	PART NO.
DS1	3	Lamp, White	Dialco	507-3916-0371-500
DS2		Same as DS1		
DS3		Same as DS1		
DS4	1	Lamp, Red	Dialco	507-3916-0371-600
M1	1	Meter, 1%	Simpson	M1521C/250045
S1	28	Switch, Toggle	C & K	CK7101
S2	2	Switch, Toggle	C & K	CK7102
S3		Same as S1		
S4	4	Switch, Pushbutton	C & K	P8121
S5		Same as S4		
S6		Same as S4		
S7		Same as S1		
S8		Same as S2		
S9		Same as S1		
S10		Switch, 12 pos, Rot	Stackpole	CS1107
S11		Same as S10		
S12		Same as S4		
S13		Same as S1		
S14		Same as S1		
S15		Same as S1		
S16		Same as S1		
S17		Same as S1		
S18		Same as S1		
S19		Same as S1		
S20		Same as S1		
S22		Same as S1		
S23		Same as S1		
S24		Same as S1		
S25		Same as S1		
S26		Same as S1		
S27		Same as S1		
S28		Same as S1		
S29		Same as S1		
S30		Same as S1		
S31		Same as S1		
S32		Same as S1		
S33		Same as S1		
S34		Same as S1		
S35		Same as S1		
S36	3	620 Ω , 1/2 W	Allen-Bradley	RC20
	1	1 k, 1/2 W	Allen-Bradley	RC20

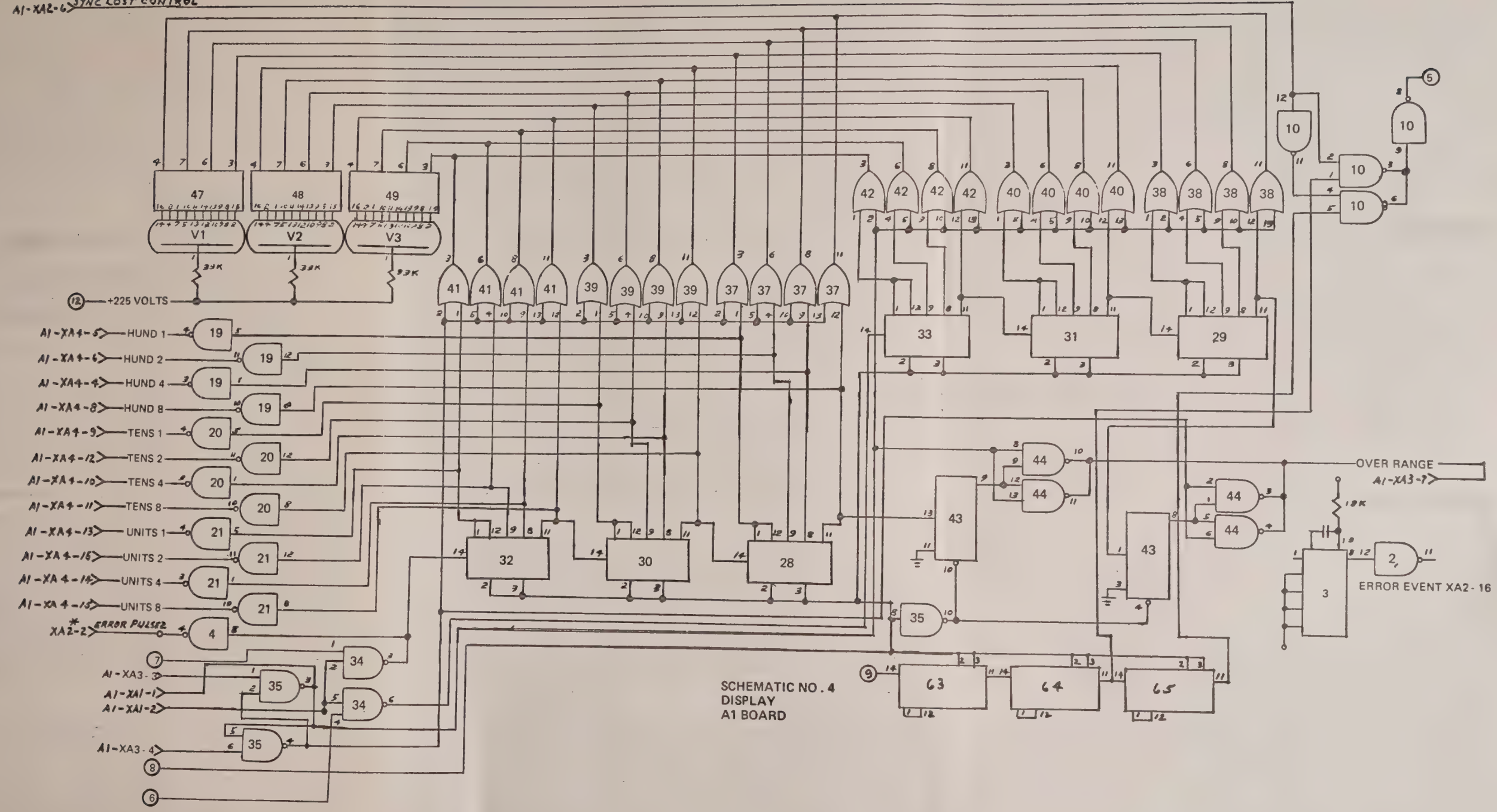


SCHEMATIC NO. 2
 TRANSMITTER LOGIC
 A1 BOARD



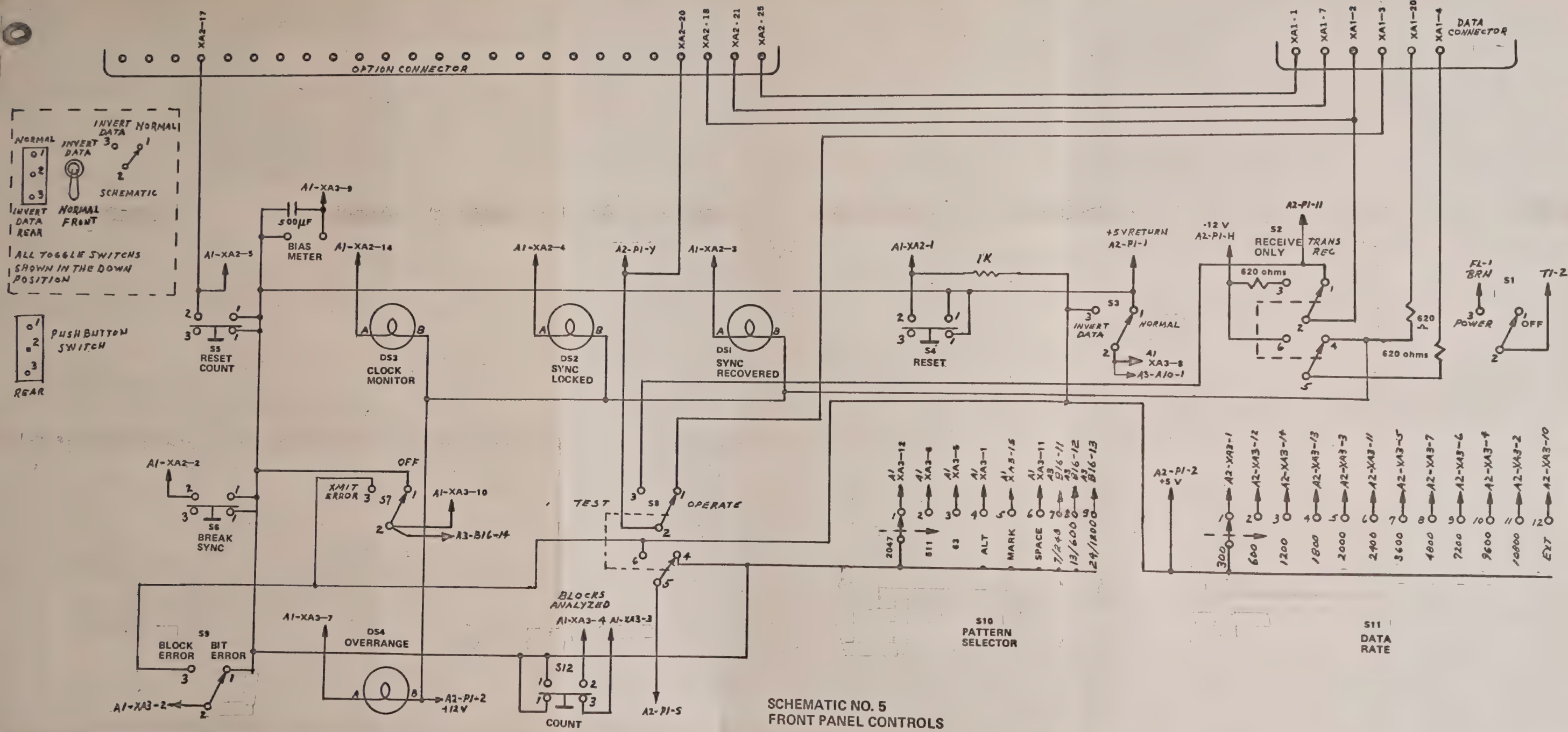
SCHEMATIC NO. 3
RECEIVER LOGIC
A1 BOARD

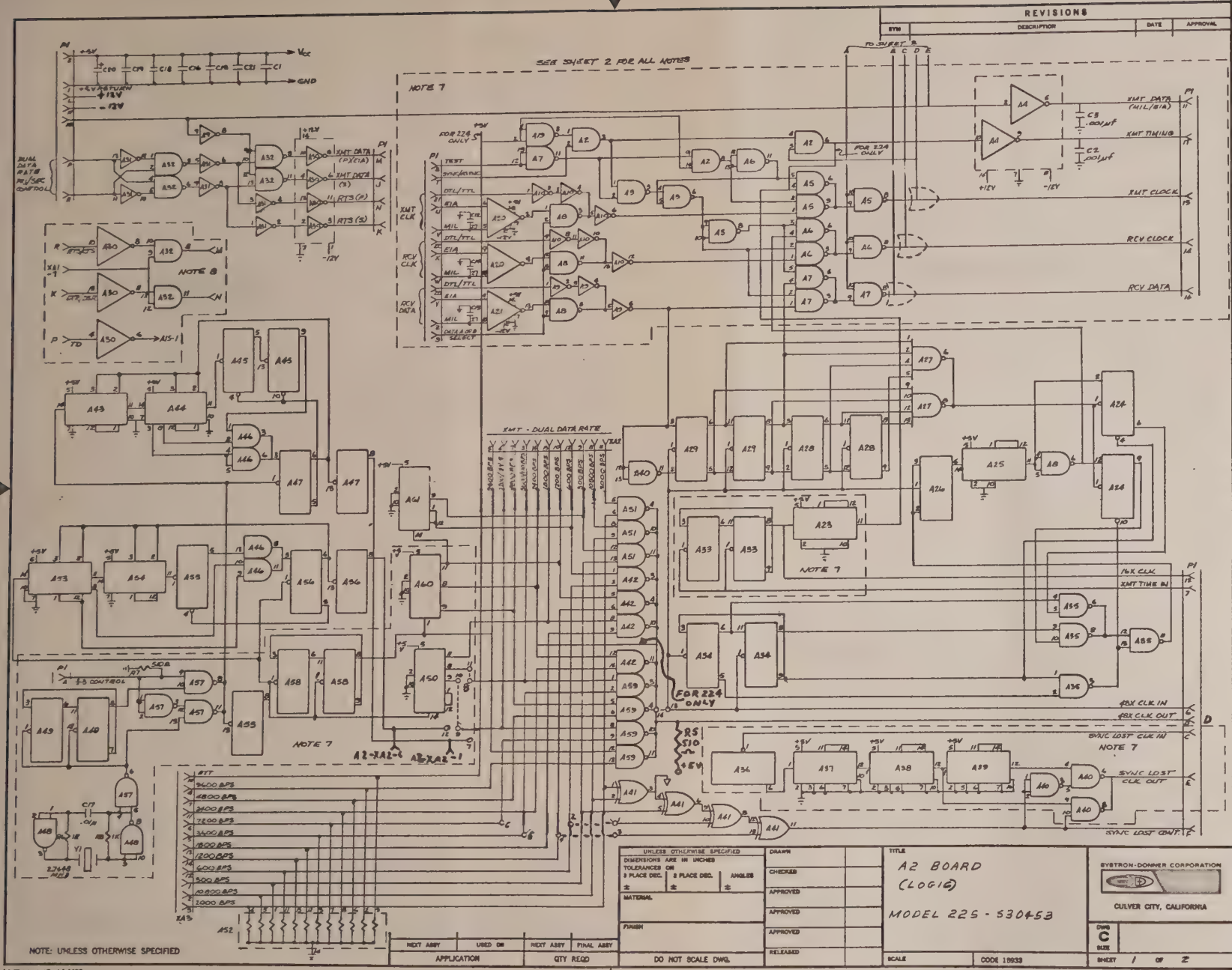
A1-XA2-6 SYNC LOST CONTROL



*OPTION CONNECTOR

3/20/74





REVISIONS

REV	DESCRIPTION	DATE	APPROVAL
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SEE SHEET 2 FOR ALL NOTES

NOTE 7

NOTE 8

NOTE 7

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
PLACE DEC. 3 PLACE DEC.
MATERIAL

DRAWN
CHECKED
APPROVED
APPROVED
APPROVED
RELEASED

TITLE
A2 BOARD
(LOGIC)
MODEL 225-530453

SYSTRON-DOMER CORPORATION
CULVER CITY, CALIFORNIA

APPLICATION	QTY REQD	DO NOT SCALE DWG.
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SCALE	CODE 19933	SHEET 1 OF 2
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REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

NOTES: APPLICABLE TO SHEETS 1 & 2

1. UNLESS OTHERWISE SPECIFIED, ALL DIP'S:

FIN 7 13 GND
PIN 14 15 Vcc

2. FOR STANDARD BOARD, CONNECT:

1 TO 2 (BUSS WIRE)
3 TO 4 (" ")
8 TO 10
8 TO 11
13 TO 14 *

3. FOR 110BPS DATA RATE, CONNECT:

7 TO 8
3 TO 5
1 TO 2
9 TO 10
15 TO 16 *

4. FOR 134.5BPS DATA RATE, CONNECT:

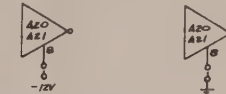
9 TO 12
1 TO 6
3 TO 7
8 TO 11
13 TO 14 *

5. FOR START/STOP OPTION, CONNECT:

7 TO 8
9 TO 12
3 TO 5
1 TO 6
15 TO 16 *

* DELETE FOR DATA SYNCHRONIZING OPTION

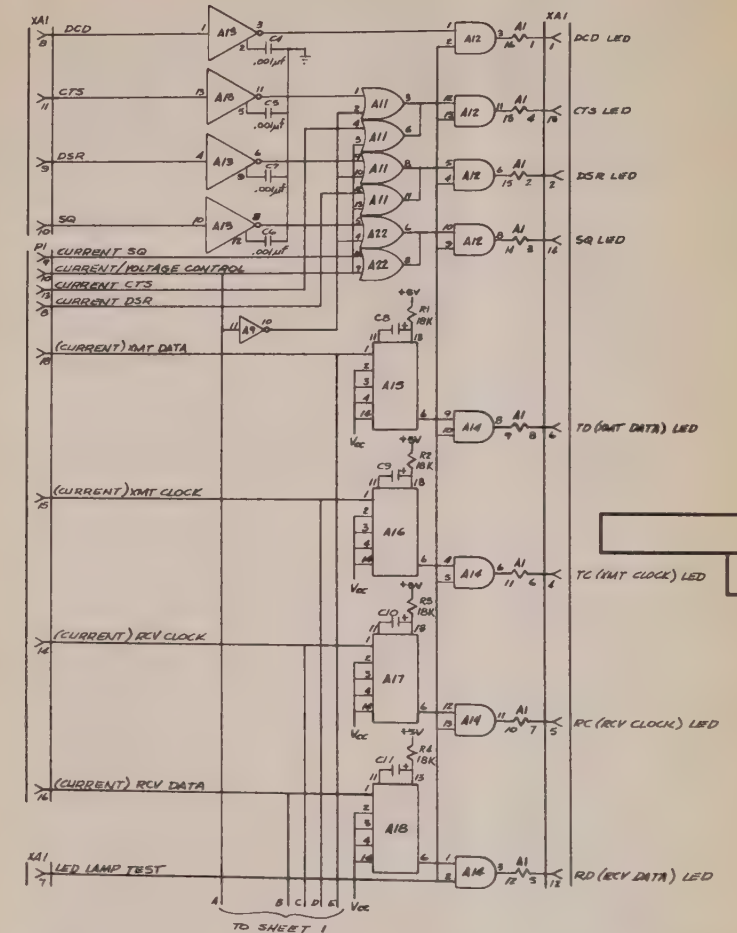
6. FOR CM1160: FOR NST16A:



7. ENCLOSED CIRCUITRY FOR 224
ADDITIONAL JUMPERS

A19-1 TO A19-14
A42-11 TO A42-12
A5-4 TO A4-10

8. ENCLOSED CIRCUITRY FOR TRANSPARENT MODE.



NOTE: UNLESS OTHERWISE SPECIFIED

INXT ARMY	USED ON	INXT ARMY	FINAL ARMY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED	DRAWN
DIMENSIONS ARE IN INCHES	CHECKED
TOLERANCES ON	ANGLES
3 PLACE DEC.	1 PLACE DEC.
MATERIAL	APPROVED
FINISH	APPROVED
	APPROVED
	RELEASED

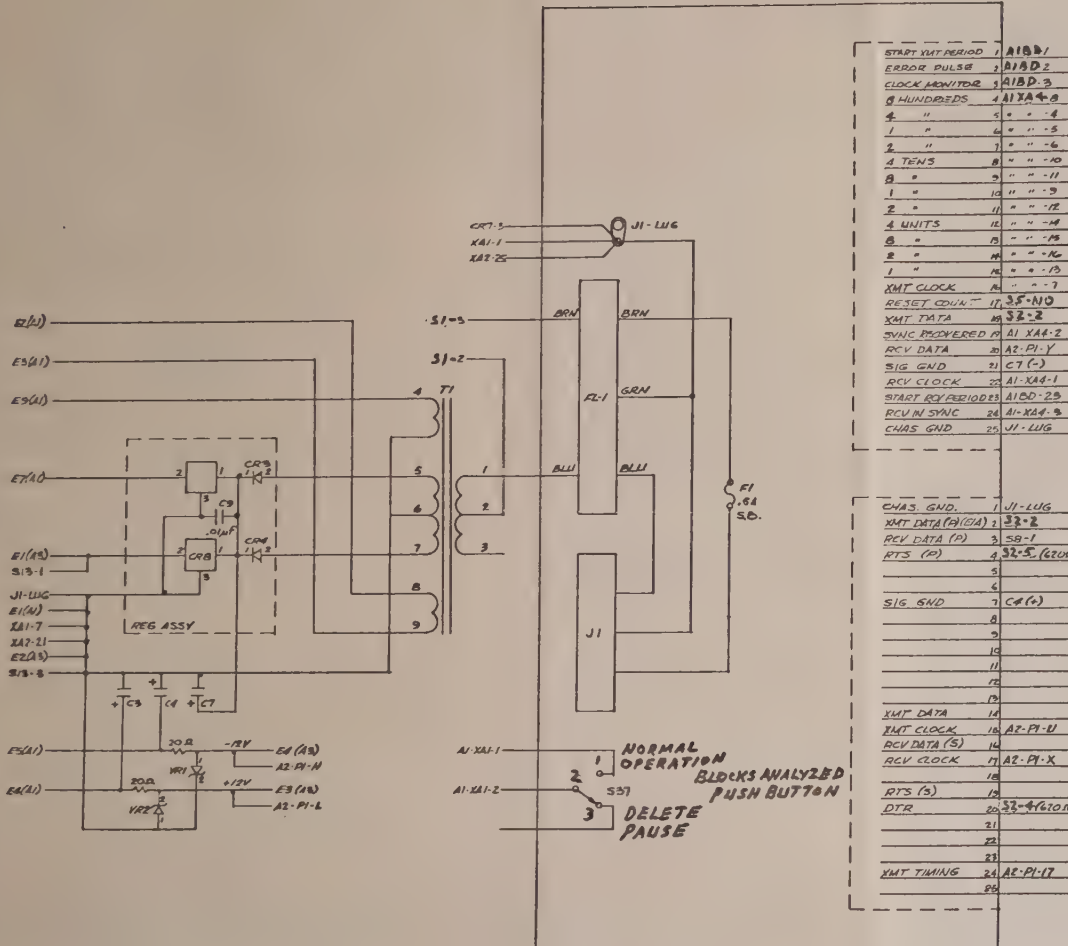
TITLE
A2 BOARD
(DISPLAY DRIVERS)
MODEL 225-530453

SYSTRON-DONNER CORPORATION
CULVER CITY, CALIFORNIA

DATE
SIZE
SHEET 2 OF 2

REVISIONS

ITEM	DESCRIPTION	DATE	APPROVAL
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START INT PERIOD	1	A100-1
ERROR PULSE	2	A100-2
CLOCK ASYNCH	3	A100-3
8 HUNDREDS	4	A100-4
7	5	A100-5
6	6	A100-6
5	7	A100-7
4 TENS	8	A100-8
3	9	A100-9
2	10	A100-10
1	11	A100-11
0	12	A100-12
9 UNITS	13	A100-13
8	14	A100-14
7	15	A100-15
6	16	A100-16
5	17	A100-17
4	18	A100-18
3	19	A100-19
2	20	A100-20
1	21	A100-21
0	22	A100-22
9 UNITS	23	A100-23
8	24	A100-24
7	25	A100-25
6	26	A100-26
5	27	A100-27
4	28	A100-28
3	29	A100-29
2	30	A100-30
1	31	A100-31
0	32	A100-32
9 UNITS	33	A100-33
8	34	A100-34
7	35	A100-35
6	36	A100-36
5	37	A100-37
4	38	A100-38
3	39	A100-39
2	40	A100-40
1	41	A100-41
0	42	A100-42
9 UNITS	43	A100-43
8	44	A100-44
7	45	A100-45
6	46	A100-46
5	47	A100-47
4	48	A100-48
3	49	A100-49
2	50	A100-50
1	51	A100-51
0	52	A100-52
9 UNITS	53	A100-53
8	54	A100-54
7	55	A100-55
6	56	A100-56
5	57	A100-57
4	58	A100-58
3	59	A100-59
2	60	A100-60
1	61	A100-61
0	62	A100-62
9 UNITS	63	A100-63
8	64	A100-64
7	65	A100-65
6	66	A100-66
5	67	A100-67
4	68	A100-68
3	69	A100-69
2	70	A100-70
1	71	A100-71
0	72	A100-72
9 UNITS	73	A100-73
8	74	A100-74
7	75	A100-75
6	76	A100-76
5	77	A100-77
4	78	A100-78
3	79	A100-79
2	80	A100-80
1	81	A100-81
0	82	A100-82
9 UNITS	83	A100-83
8	84	A100-84
7	85	A100-85
6	86	A100-86
5	87	A100-87
4	88	A100-88
3	89	A100-89
2	90	A100-90
1	91	A100-91
0	92	A100-92
9 UNITS	93	A100-93
8	94	A100-94
7	95	A100-95
6	96	A100-96
5	97	A100-97
4	98	A100-98
3	99	A100-99
2	100	A100-100

CHAS. GND.	1	J1-LUG
XMT DATA (H/DA)	2	32-2
RCV DATA (P)	3	58-1
RTS (P)	4	32-5 (GND)
5	5	
6	6	
SIG. GND	7	C6-1
8	8	
9	9	
10	10	
11	11	
12	12	
13	13	
14	14	
XMT DATA	15	A2-PI-U
INT. CLOCK	16	A2-PI-U
RCV DATA (S)	17	A2-PI-X
RCV CLOCK	18	A2-PI-X
19	19	
RTS (S)	20	32-4 (GND)
DTR	21	
22	22	
23	23	
XMT TIMING	24	A2-PI-17
25	25	

NORMAL OPERATION
BLOCKS ANALYZED
PUSH BUTTON
DELETE PAUSE

NOTE: UNLESS OTHERWISE SPECIFIED

REV	APP	USED OR	REV	APP	FINAL
1	1	1	1	1	1

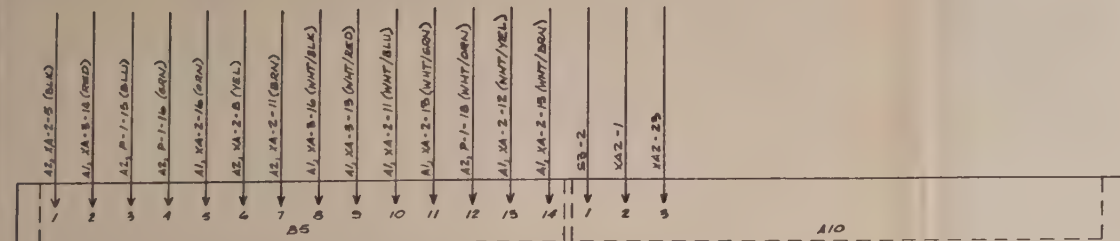
UNLESS OTHERWISE SPECIFIED		
DIMENSIONS ARE IN INCHES		
TOLERANCES ON		
3 PLACE DEC.	2 PLACE DEC.	ANGLES
±	±	±
MATERIAL		
FINISH		
APPROVED		
RELEASED		

TITLE	
INTERCONNECTION (POWER/SIGNAL) MODEL 225-530453	

BYSTRON-DOPHER CORPORATION	
CULVER CITY, CALIFORNIA	
DATE	REV
10/1/78	1
SHEET 01	

3/20/74

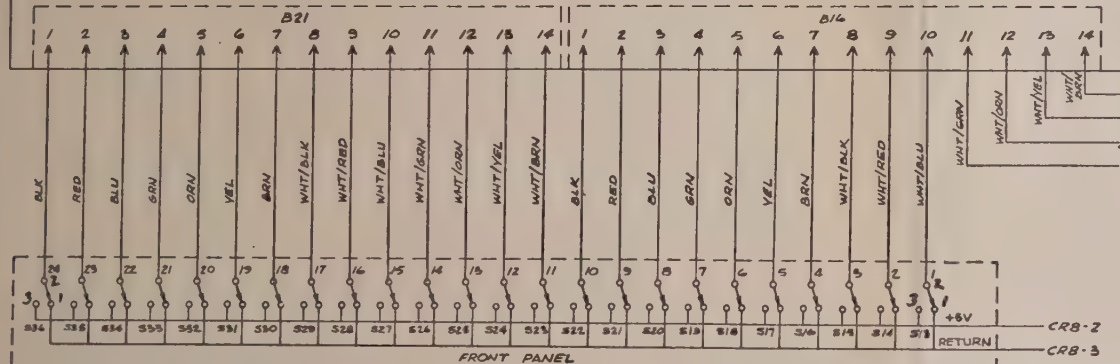
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



A10 BOARD

FRAME GND		
6	(YEL)	300 B/S CLK (WTR)
5	(ORN)	600 B/S " "
4	(GRN)	1200 B/S " "
3	(WHT/RED)	1800 B/S " "
10	(WHT/BLU)	2000 B/S " "
		SIG GND
3	(BLU)	2400 B/S CLK (WTR)
8	(WHT/BLK)	3600 B/S " "
2	(RED)	4800 B/S " "
7	(BRN)	7200 B/S " "
1	(BLK)	9600 B/S " "
11	(WHT/GRN)	10800 B/S " "
12	(WHT/ORN)	EXT XMT CLK
13	(WHT/YEL)	XMT FRAME SYNC
14	(WHT/BRN)	RCV FRAME SYNC

EIA CONN
(DB-255)



TOGGLE SWITCHES SHOWN
IN THE DOWN POSITION

NOTE: UNLESS OTHERWISE SPECIFIED

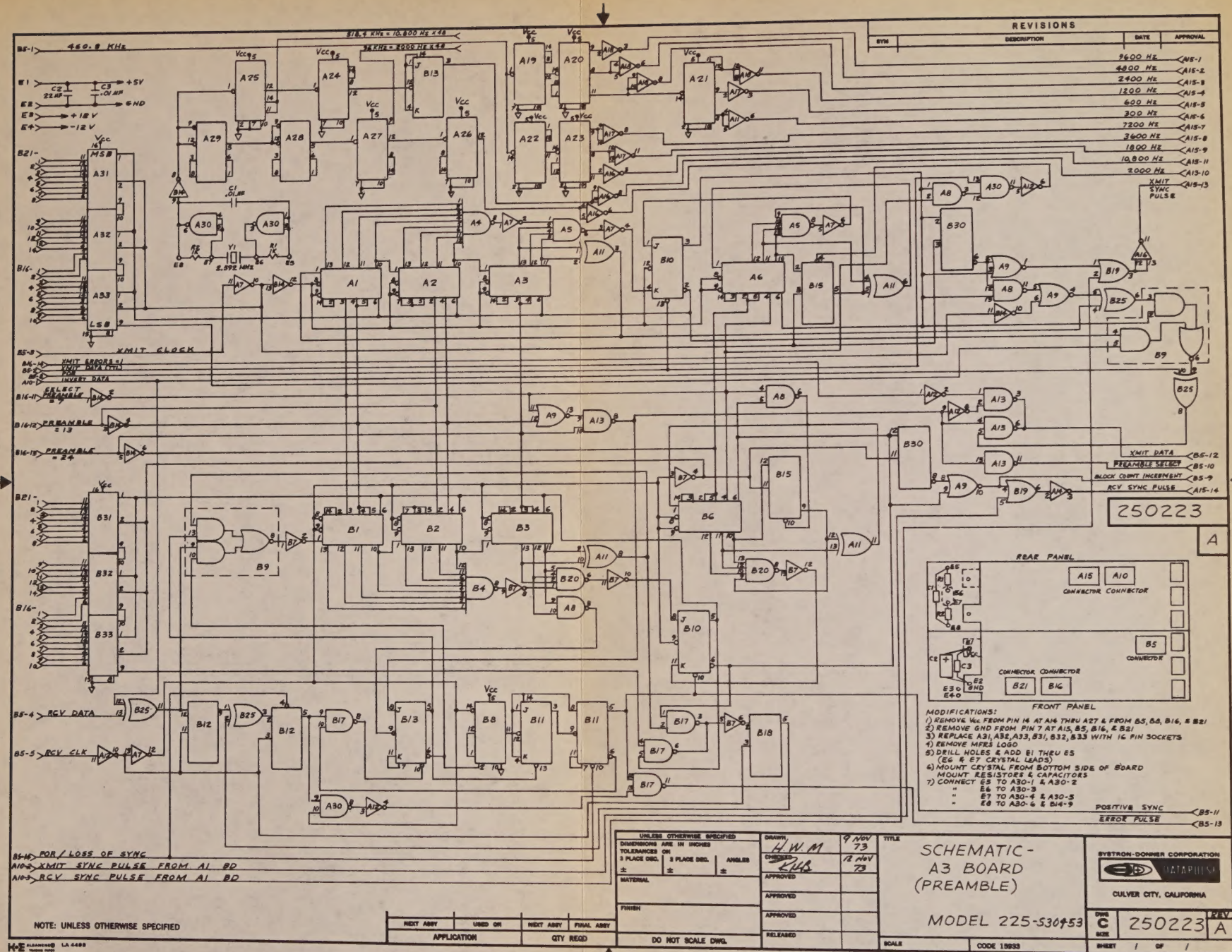
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED		
DIMENSIONS ARE IN INCHES		
TOLERANCES ON		
1 PLACE DEC.	2 PLACE DEC.	ANGLES
±	±	±
MATERIAL		
FINISH		

DRAWN	
CHECKED	
APPROVED	
APPROVED	
APPROVED	
RELEASED	

TITLE	
INTERCONNECTION	
MODEL 225-530453	
SCALE	
CODE 19233	

SYSTEM-DOHMER CORPORATION	
CULVER CITY, CALIFORNIA	
DWG C	
SHEET	OF



WARRANTY

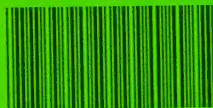
The Datapulse Division, Systron-Donner Corporation (hereinafter referred to as Datapulse) warrants each instrument of its manufacture to be free from defects in material and workmanship. Our obligation under this Warranty is limited to servicing or adjusting any instrument returned to our factory for that purpose, and to making good at our factory any part or parts thereof except tubes, transistors, fuses or batteries which shall, within one year after making delivery to the original purchaser, be returned to us with transportation charges prepaid, and which our examination shall disclose to our satisfaction to have been thus defective.

Instruments returned under this Warranty will not be accepted at the Datapulse plant without prior authorization by a Datapulse representative or by the service manager of Datapulse.

Datapulse reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This Warranty is expressly in lieu of all other obligations or liabilities on the part of Datapulse and Datapulse neither assumes nor authorizes any other person to assume for them any other liability in connection with the sales of Datapulse instruments.

MP MASTER



MA28866